Digital Integrated Circuit Design

CMPE 530/630

# Power Consumption

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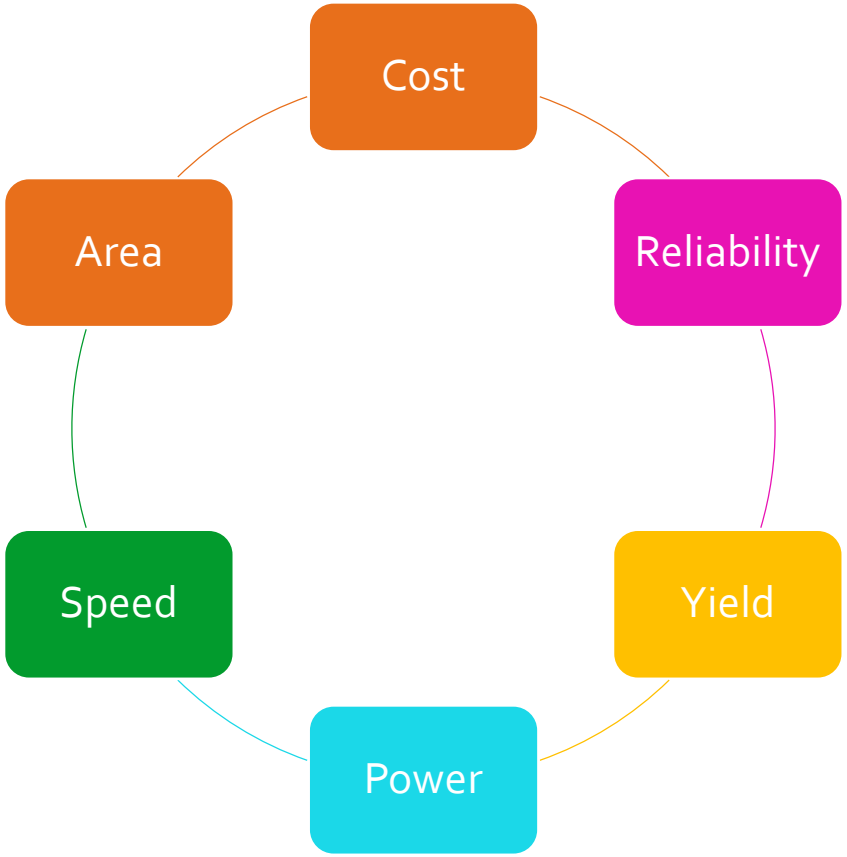
# Learning Objectives

- Be able to describe the primary components of power consumption in CMOS circuits
- Be able to estimate the power consumption of CMOS gates
- Be able to discuss how power consumption can be optimized by modifying voltages, frequencies, activity factors, etc.

# Evaluating Digital ICs

- What are the tradeoffs?
- What influences what?



# What is Power?

- Power is the rate of work:

$$P(t) \equiv \frac{\mathrm{d}W}{\mathrm{d}t}$$

- Voltage is the work per unit charge

$$v(t) \equiv \frac{W}{Q}$$

- Instantaneous power dissipated by a circuit element is:

$$P(t) = v(t)\frac{\mathrm{d}Q}{\mathrm{d}t} = v(t)i(t)$$

# Energy and Average Power

» Energy is the time integral of power:

$$E = \int_0^T P(t)\mathrm{d}t$$

» Average power is energy over time:

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)\mathrm{d}t$$

# Power in Resistors and Capacitors

» Resistors (using Ohm's law):

$$P_R = vi = i^2 R = \frac{v^2}{R}$$

» Capacitors (using $Q = vC$):

$$E_C = \int_0^\infty v(t)i(t)\mathrm{d}t = \int_0^\infty C\frac{\mathrm{d}v(t)}{\mathrm{d}t}v(t)\mathrm{d}t = C\int_0^{V_C} v(t)\mathrm{d}v = \frac{1}{2}CV_C^2$$

» Power supplies:

$$P_{Vdd}(t) = V_{dd}i_{dd}(t)$$

# Components of Power Consumption

- Total power consumption is composed of two main components:

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$$

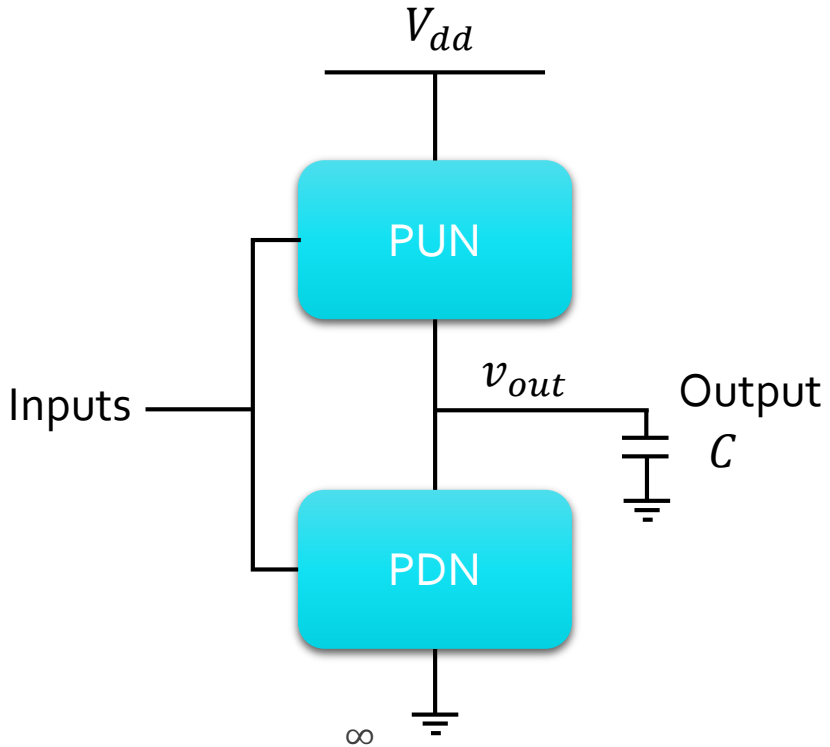
- Dynamic power is consumed when the circuit is "doing something"

- Static power is consumed when the circuit is idle

# Dynamic Power Consumption

$$P_{dynamic} = P_{\text{switching}} + P_{\text{short circuit}} + P_{\text{glitch}}$$

» Dynamic power is primarily caused by gates switching:




$$P_{\text{switching}} = \frac{1}{T}\int_0^{\infty} V_{dd} i_{dd}(t)\mathrm{d}t = \frac{1}{T}\int_0^{\infty} V_{dd} C \frac{\mathrm{d}v_{out}}{\mathrm{d}t}\,\mathrm{d}t = \frac{1}{T} C V_{dd} \int_0^{V_{dd}} \mathrm{d}v_{out} = \frac{1}{T} C V_{dd}^2$$

# Dynamic Power Consumption

- Notice that the energy stored by the load capacitor is only half of the total switching energy
  - Half of the energy goes to power dissipation through either the PUN or PDN!
    - "Reversible computing" methodologies seek to reduce or eliminate power consumption by shuffling energy around instead of resupplying it from $V_{dd}$ or ground

- Our switching period $T$ is related to the operating frequency as: $T = \alpha / f$, where $a$ is the "activity factor":

$$P_{\text{switching}} = \alpha C V_{dd}^2 f$$

- $\alpha$ is the probability that a gate will switch from 0 to 1 within $T$

# Switching Activity Factor

» Switching activity factor is calculated as:

$$\alpha = \Pr(\text{output} = 0)\Pr(\text{output} = 1) = \overline{P}_Y P_Y = (1 - P_Y)P_Y$$

» Clocks have $\alpha = 1$

» $\alpha = 0.1$ often used for estimation

» Exact activity factors requires simulation

| Gate | $P_Y$ | $\alpha$ (assuming inputs with $P_Y = 0.5$) |
|---|---|---|
| AND2 | $P_A P_B$ | 3/16 |
| AND3 | $P_A P_B P_C$ | 7/64 |
| OR2 | $1 - \overline{P}_A \overline{P}_B$ | 3/16 |
| NAND2 | $1 - P_A P_B$ | 3/16 |
| NOR2 | $\overline{P}_A \overline{P}_B$ | 3/16 |
| XOR2 | $P_A \overline{P}_B + \overline{P}_A P_B$ | 1/4 |

# Other Dynamic Power Components

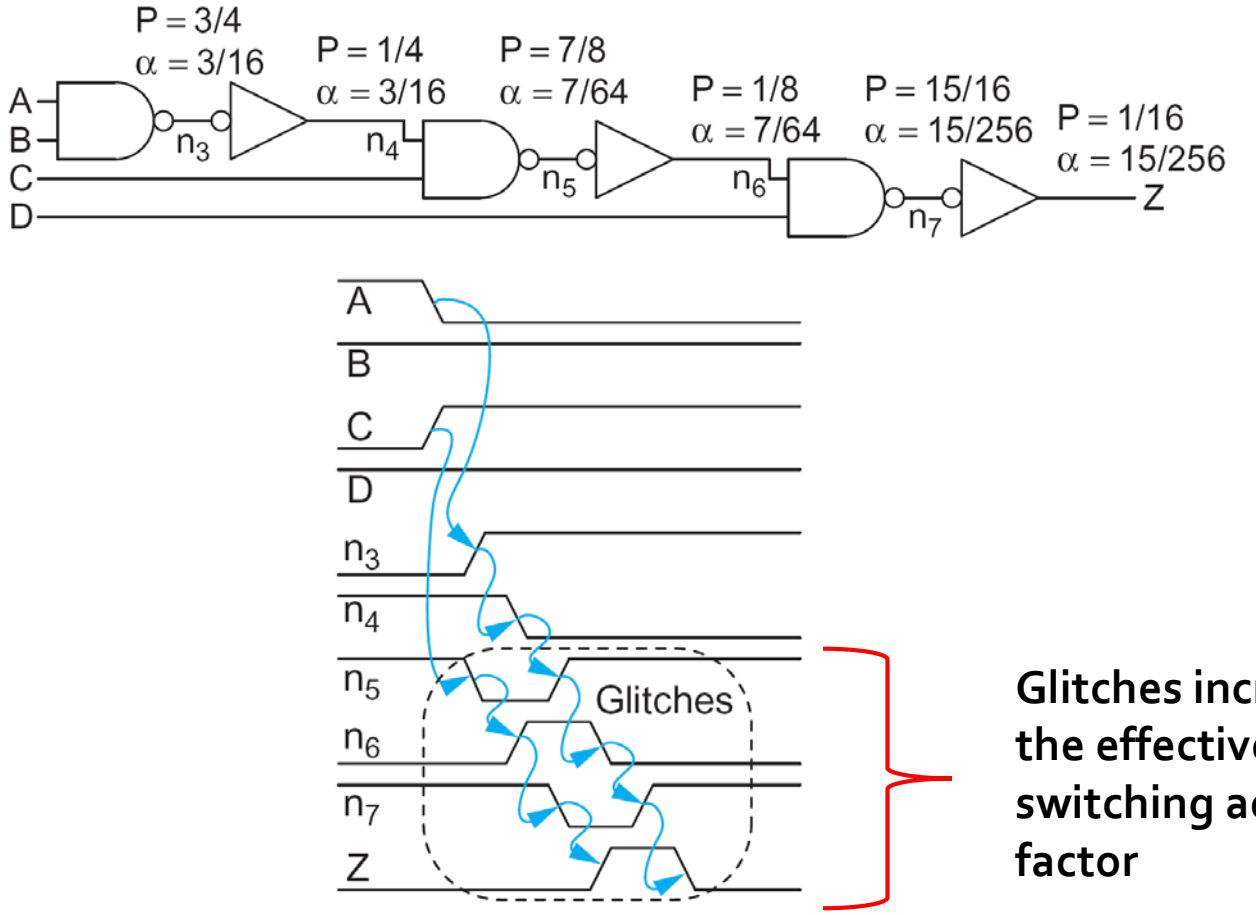
- During switching, there may be a short period of time that both the PUN and PDN are on
  - Power consumed during this time is called short-circuit power

- Function of $V_t/V_{dd}$
  - When >0.5, $P_{\text{short circuit}} = 0$
  - Otherwise, typically 2%-10% of switching power

- Function of input rise/fall times
  - Slower inputs cause higher short circuit power

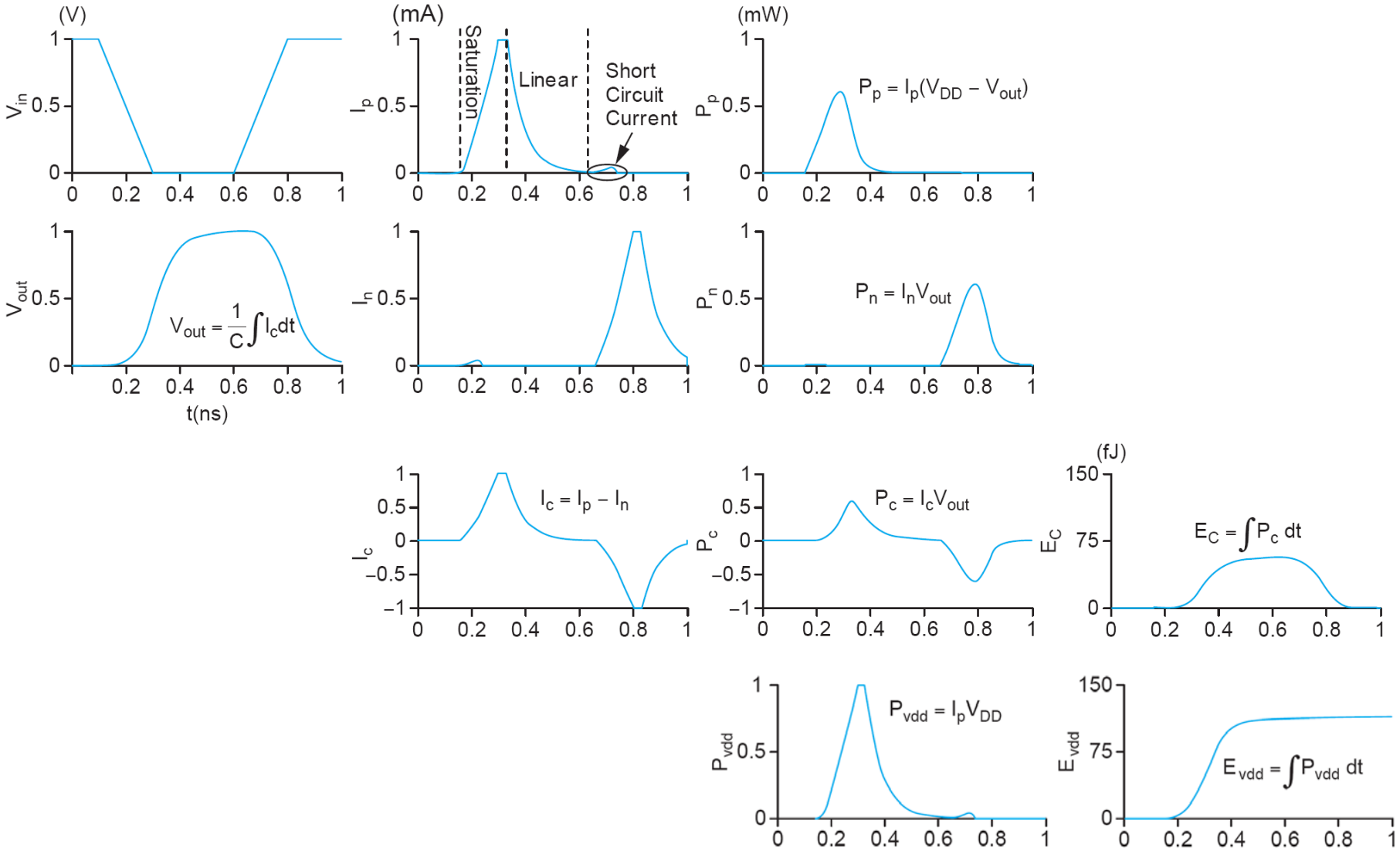
# Other Dynamic Power Components

» Additional power can be consumed when hazards are present in the circuits, causing "glitches":




**Glitches increase the effective switching activity factor**

# Inverter Dynamic Power



# Methods for Reducing Dynamic Power Consumption

» Recall most of dynamic power comes from switching:

$$P_{\text{switching}} = \alpha C V_{dd}^2 f$$

» Reduce $\alpha$
- Clock/power gating

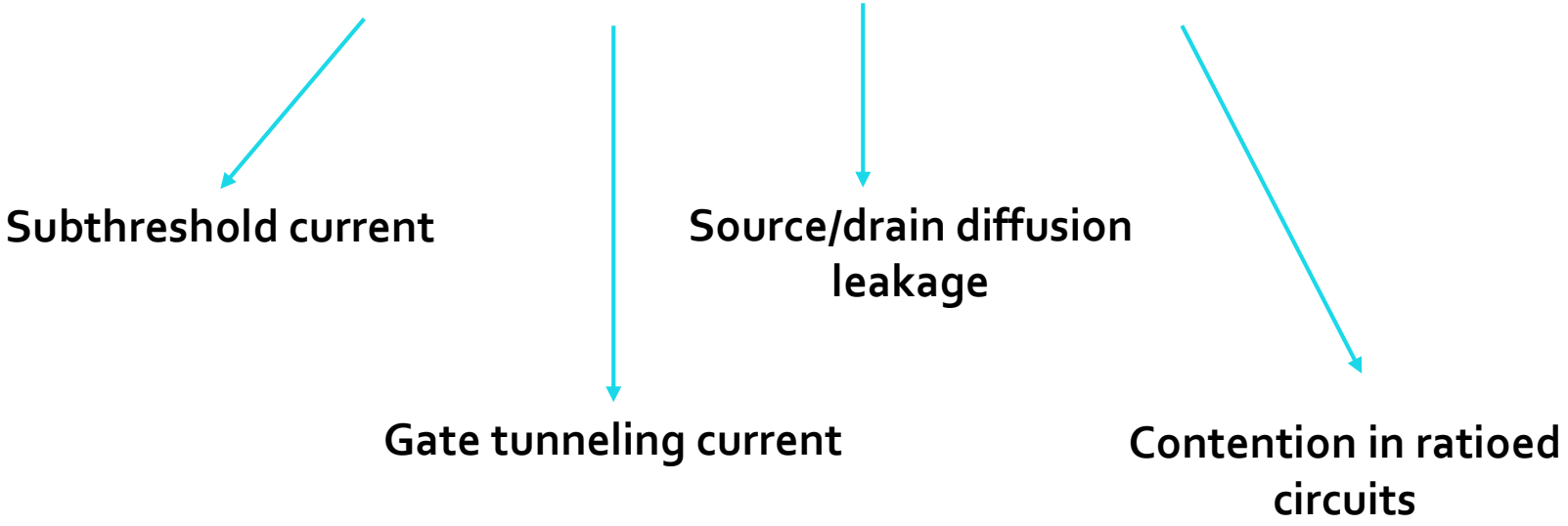
» Reduce $C$
- Smaller transistors, better materials

» Reduce $V_{dd}$ and $f$
- Dynamic voltage/frequency scaling

# Static Power Consumption

» Static power consumption occurs when circuits are idle

$$P_{static} = (I_{sub} + I_{gate} + I_{junct} + I_{contention})V_{dd}$$




» Large static power has led to the era of "dark silicon"

- Large portion of circuit has to be disconnected from supply at any given time to meet power constraints

# Static Power Consumption

- Subthreshold leakage
  - Even when $V_{gs} < V_{th}$, current flows due to diffusion

**DIBL Coefficient** **Body Effect Coefficient**

$$I_{sub} = \beta V_T^2 (n-1) e^{\frac{V_{eff} + \eta(V_{ds} - V_{dd}) - k_\gamma V_{sb}}{nV_T}} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right)$$

- Static power reduction techniques
  - Transistor stacking
    - Series transistors have less leakage
  - Power gating
    - Use transistor to cut off the supply to a particular circuit
  - Multiple threshold voltages
    - Use higher threshold in non-critical paths

# Shrinking Transistor Sizes

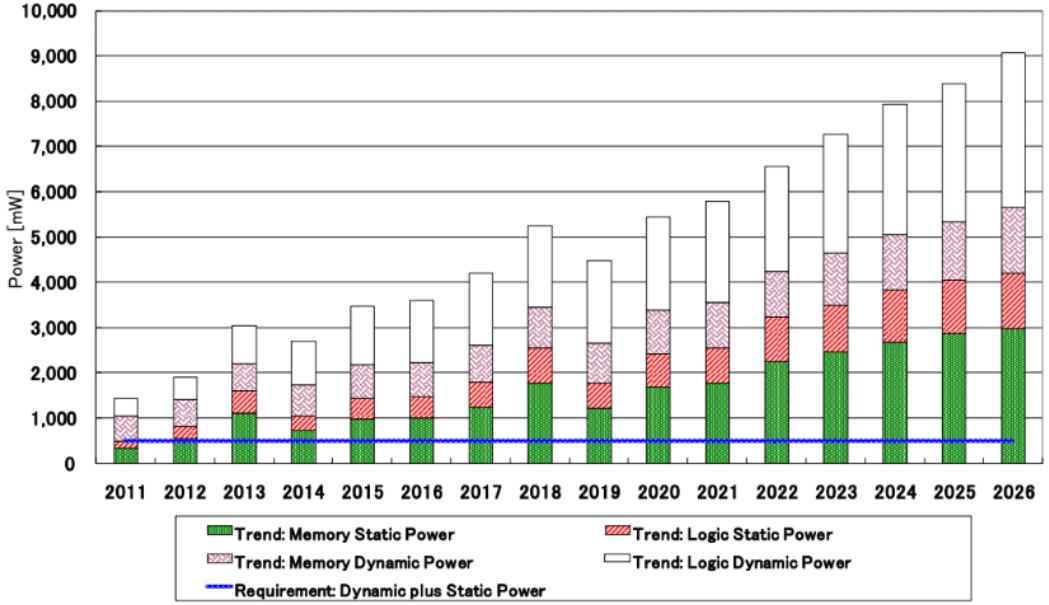
» Why does the IC industry want to scale?

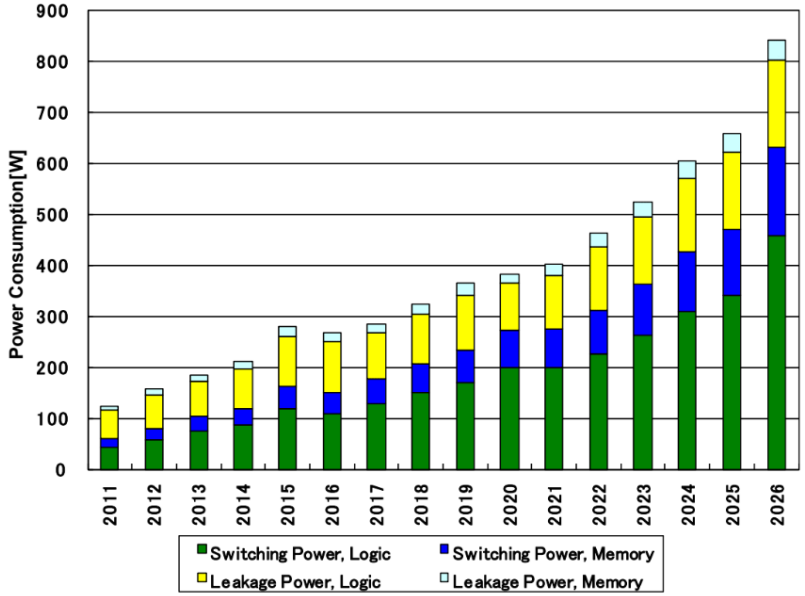
| Parameter | Sensitivity | Dennard Scaling | Constant Voltage | Lateral Scaling |
|---|---|---|---|---|
| L: Length | | 1/S | 1/S | 1/S |
| W: Width | | 1/S | 1/S | 1 |
| $t_{ox}$: gate oxide thickness | | 1/S | 1/S | 1 |
| $V_{DD}$: supply voltage | | 1/S | 1 | 1 |
| $V_t$: threshold voltage | | 1/S | 1 | 1 |
| NA: substrate doping | | S | S | 1 |
| $\beta$ | $W/(Lt_{ox})$ | S | S | S |
| $I_{on}$: ON current | $\beta(V_{DD}-V_t)^2$ | 1/S | S | S |
| R: effective resistance | $V_{DD}/I_{on}$ | 1 | 1/S | 1/S |
| C: gate capacitance | $WL/t_{ox}$ | 1/S | 1/S | 1/S |
| $\tau$: gate delay | RC | 1/S | $1/S^2$ | $1/S^2$ |
| f: clock frequency | $1/\tau$ | S | $S^2$ | $S^2$ |
| E: switching energy / gate | $CV_{DD}^2$ | $1/S^3$ | 1/S | 1/S |
| P: switching power / gate | Ef | $1/S^2$ | S | S |
| A: area per gate | WL | $1/S^2$ | $1/S^2$ | 1 |
| Switching power density | P/A | 1 | $S^3$ | S |
| Switching current density | $I_{on}/A$ | S | $S^3$ | S |

Faster, more energy-efficient chips @ lower cost

# Adverse Effects of Scaling

» Power Consumption




Source: ITRS

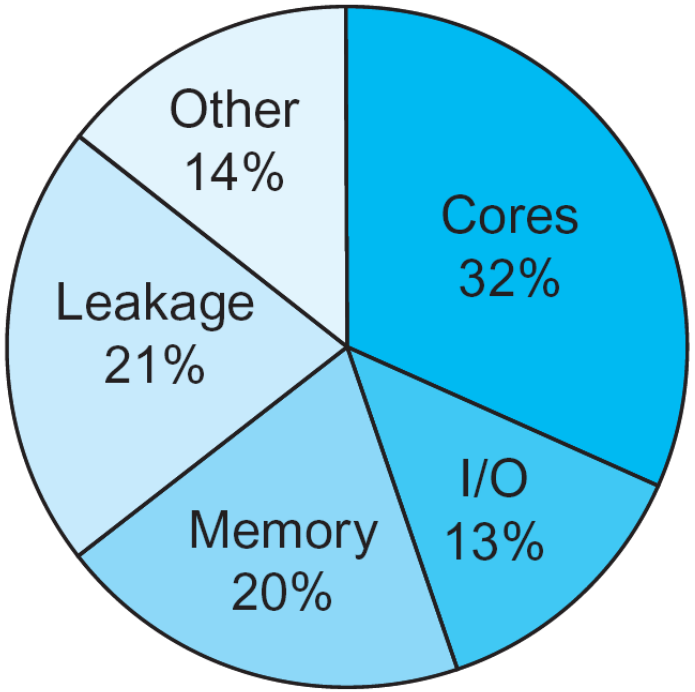
» More transistors/chip → More dynamic power

» As threshold voltages are reduced, transistors become more "leaky"

- Large static power consumption

# Division of Power in Chip

» Example from a Sun 8-core processor ("Niagra2")



# The Death of Moore's Law ☹