

Digital Integrated Circuit Design
CMPE 530/630

Introduction to Digital IC Design

Dr. Cory Merkel



A Little Bit About Me

- » From Rochester Area
- » Ph.D. in Microsystems Engineering @ RIT
- » 3 years at Air Force Research Lab
- » Research Interests:
 - Brain-inspired/neuromorphic computing
 - AI at the Edge

IC Design Flow

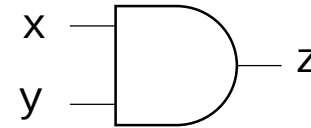
Design Specification

"I need a chip that multiplies two 1-bit numbers."

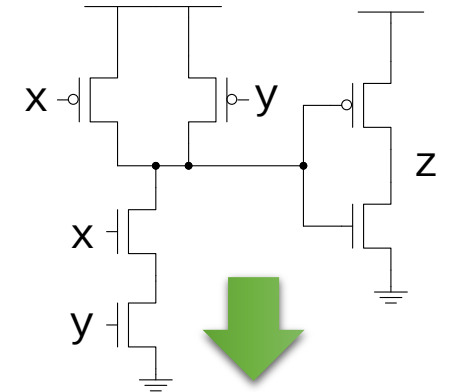
Functional Design

```
module my_chip(x,y,z);  
  input x,y,z;  
  assign z=x&y;  
endmodule
```

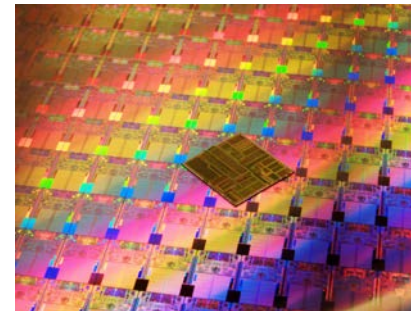
Logic Level Design



Transistor Level Design

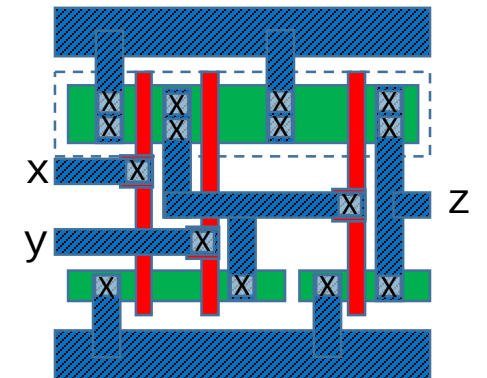


Fabrication



Source: Intel

Mask Design



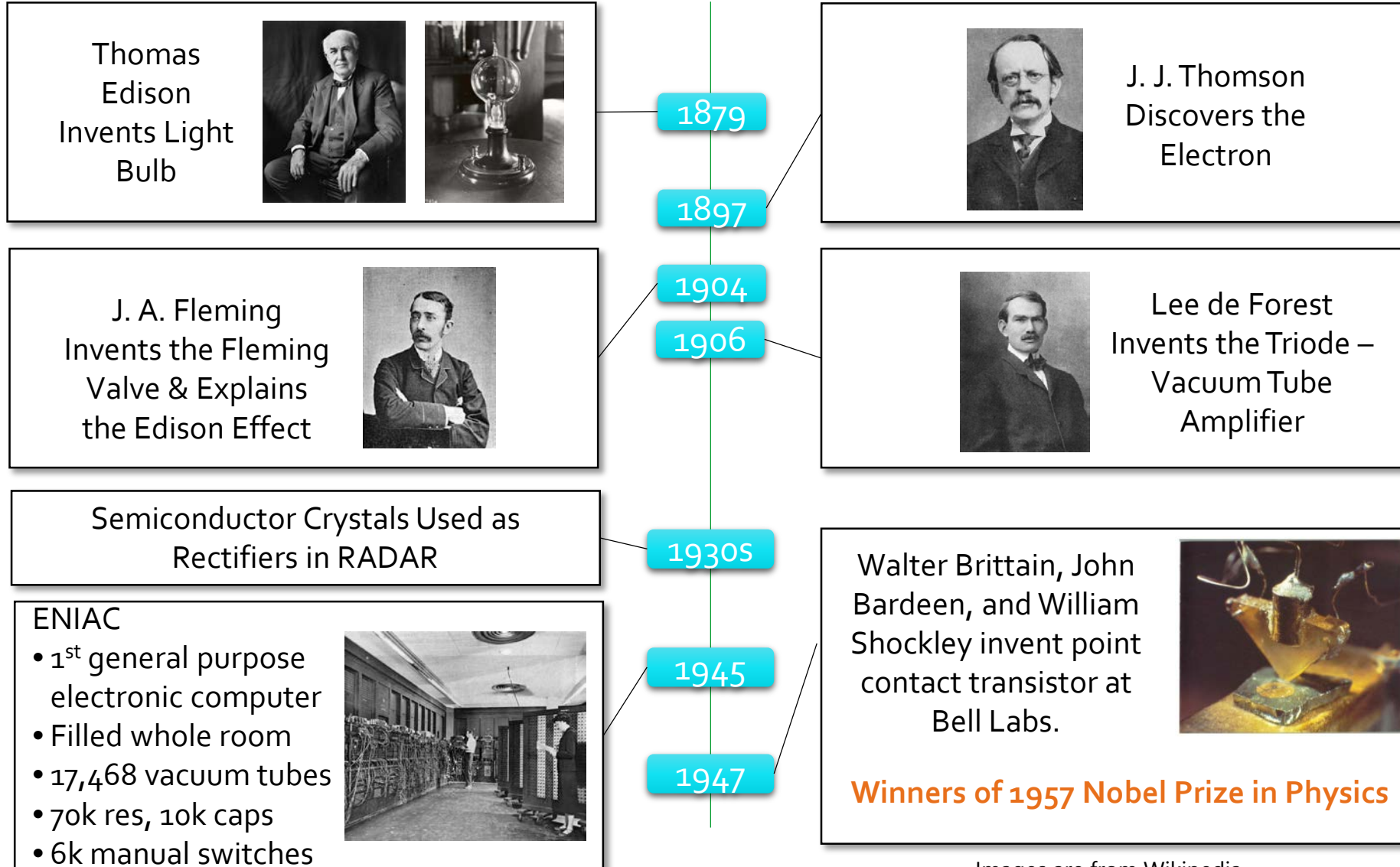
» Lots of intermediate steps not shown!

Course Goals

- » Introduce students to IC design techniques
- » Provide a strong foundation for students to explore advanced concepts on their own
- » By the end of the course, students will be able to design custom integrated circuits from concept through tapeout!

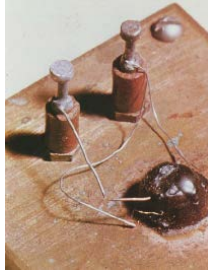


A Little History...



A Little History...

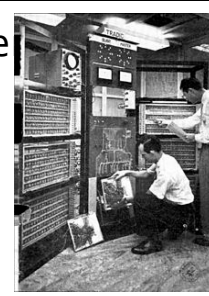
First junction transistor
invented by William
Shockley at Bell Labs



1948

TRADIC – 1st transistorized computer

- 3 cubic feet (ENIAC was 1000 ft²)
- 800 point-contact transistors
- 10k germanium crystal rectifiers
- 1M ops/sec @ < 100 W



1954

Bob Noyce
Fairchild -1st
useful integrated
circuit and planar
process.



1958

1960

1974

⋮

First integrated
circuit 3-transistor
phase-shift
oscillator invented
by Jack Kilby at TI



Winner of 2000 Nobel Prize in Physics

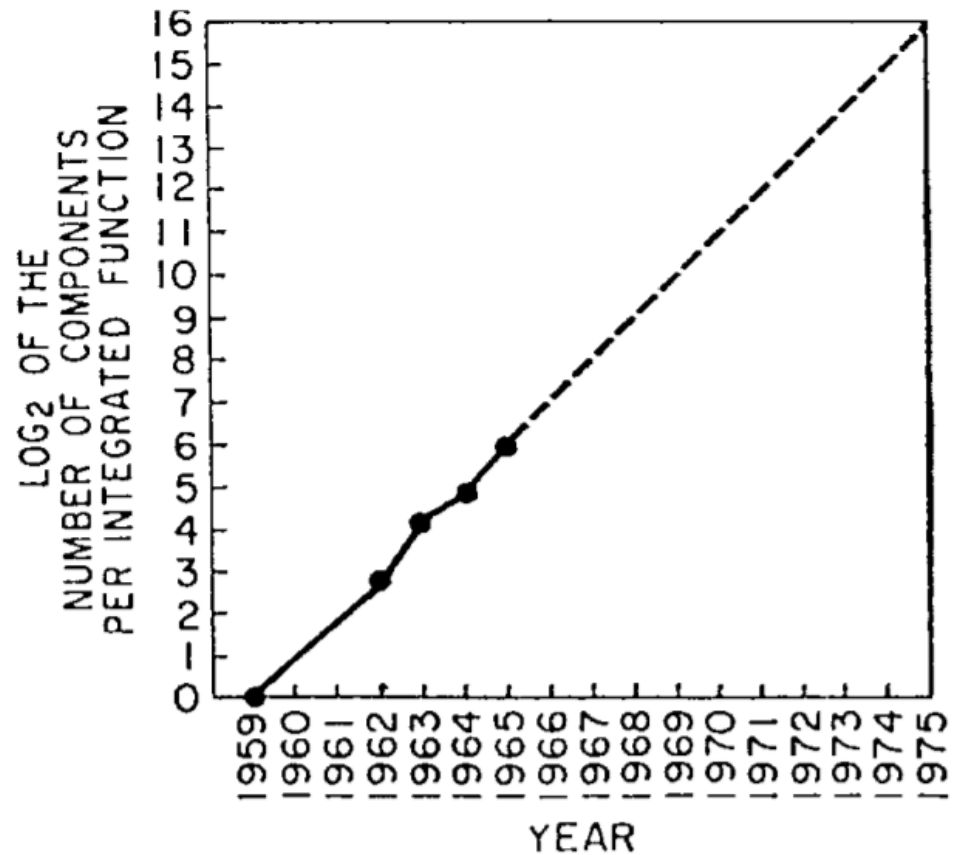
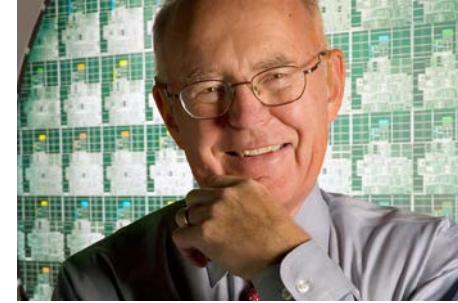
Images are from Wikipedia

» Why Integration?

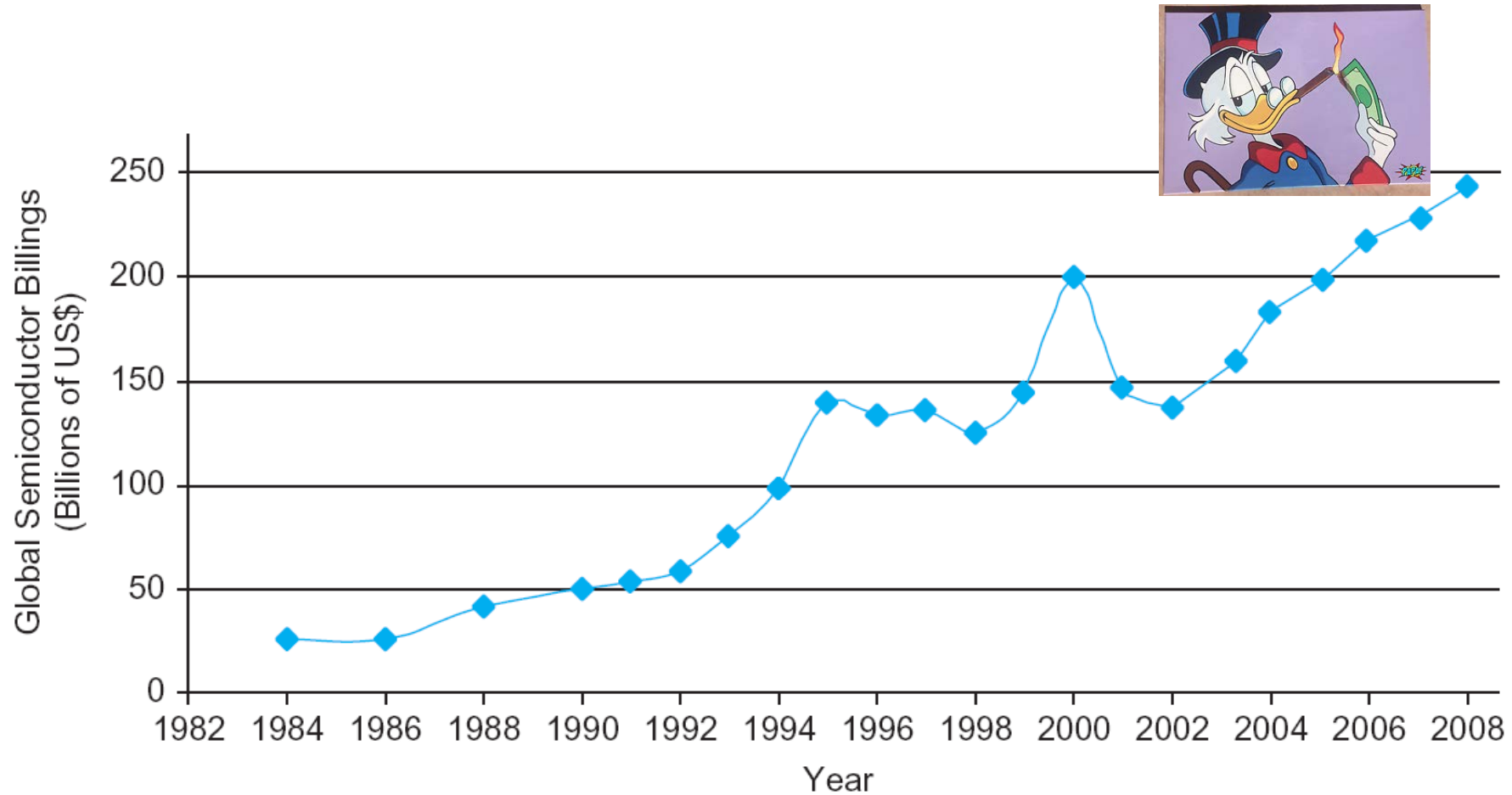
- Overcame the “tyranny of numbers”
 - Before ICs, Had to wire million of connections by hand
- Enabled unparalleled growth in IC industry for 50+years

Moore's Law and Scaling

- » 1965 – Gordon Moore: “Cramming More Components onto Integrated Circuits,”



Size of Worldwide Semiconductor Market

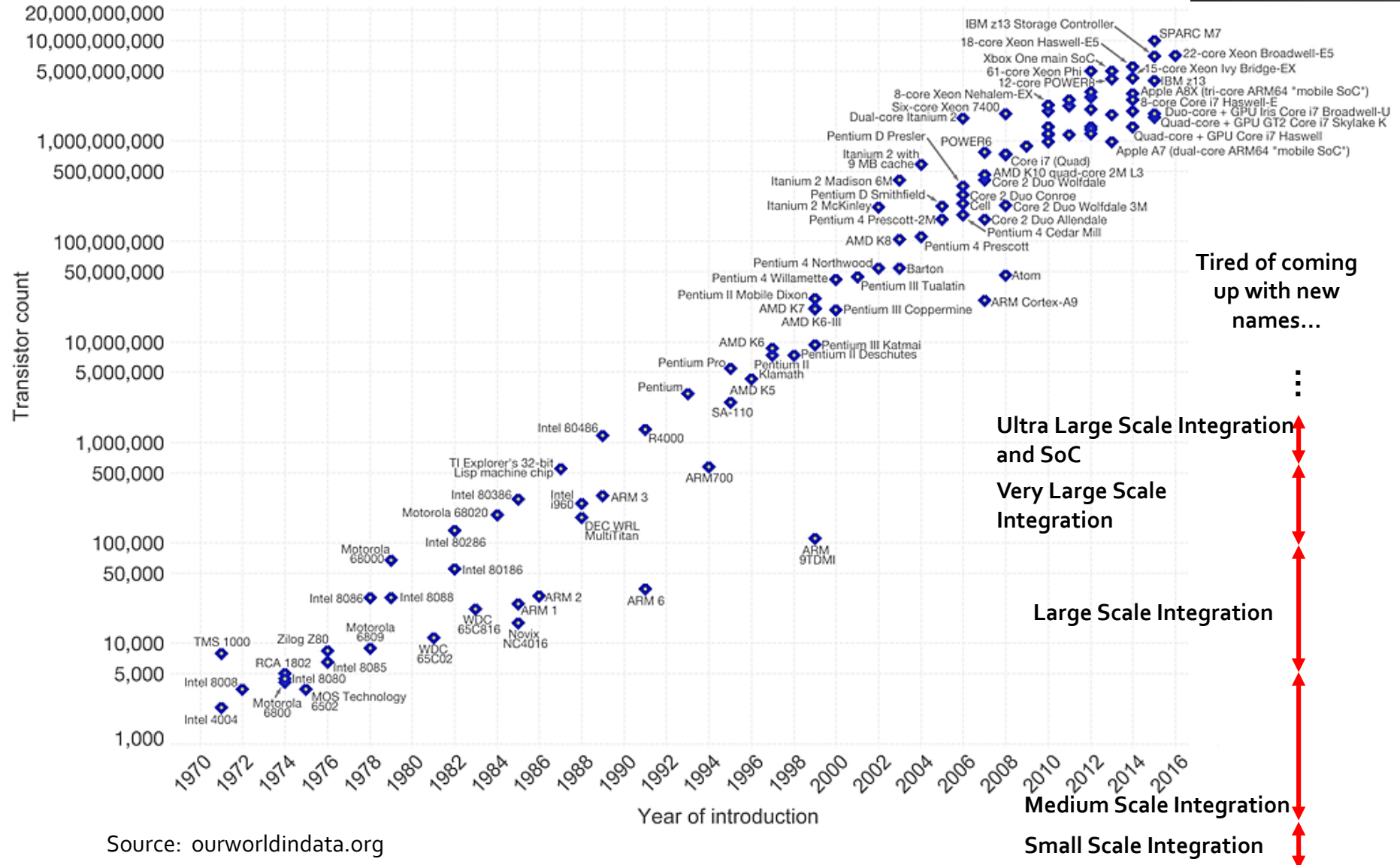
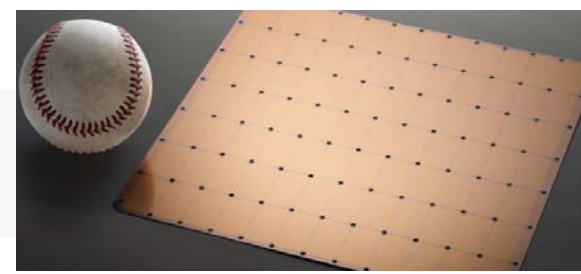


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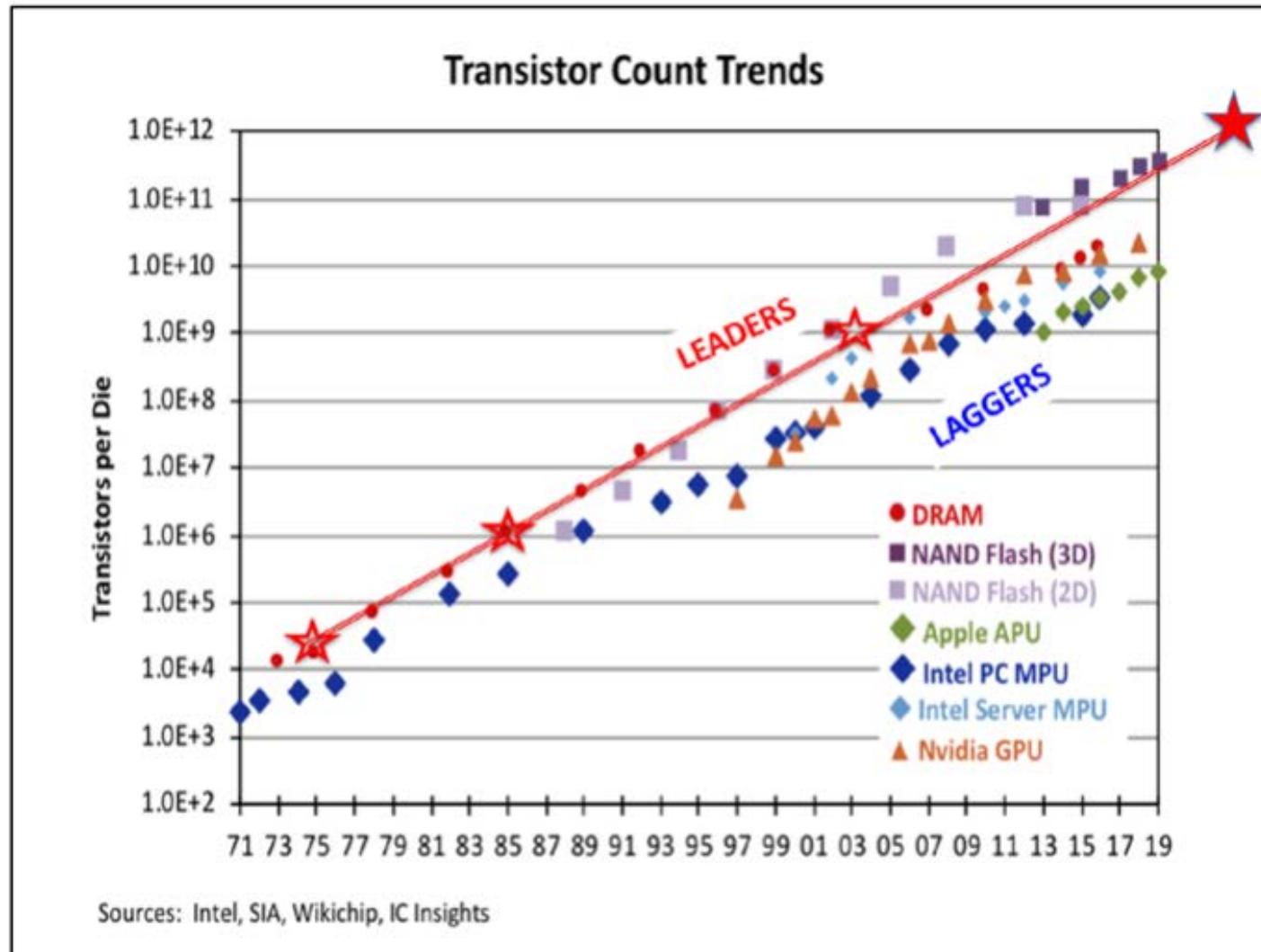
» Currently valued at over 0.5 Trillion dollars!

Transistor Counts

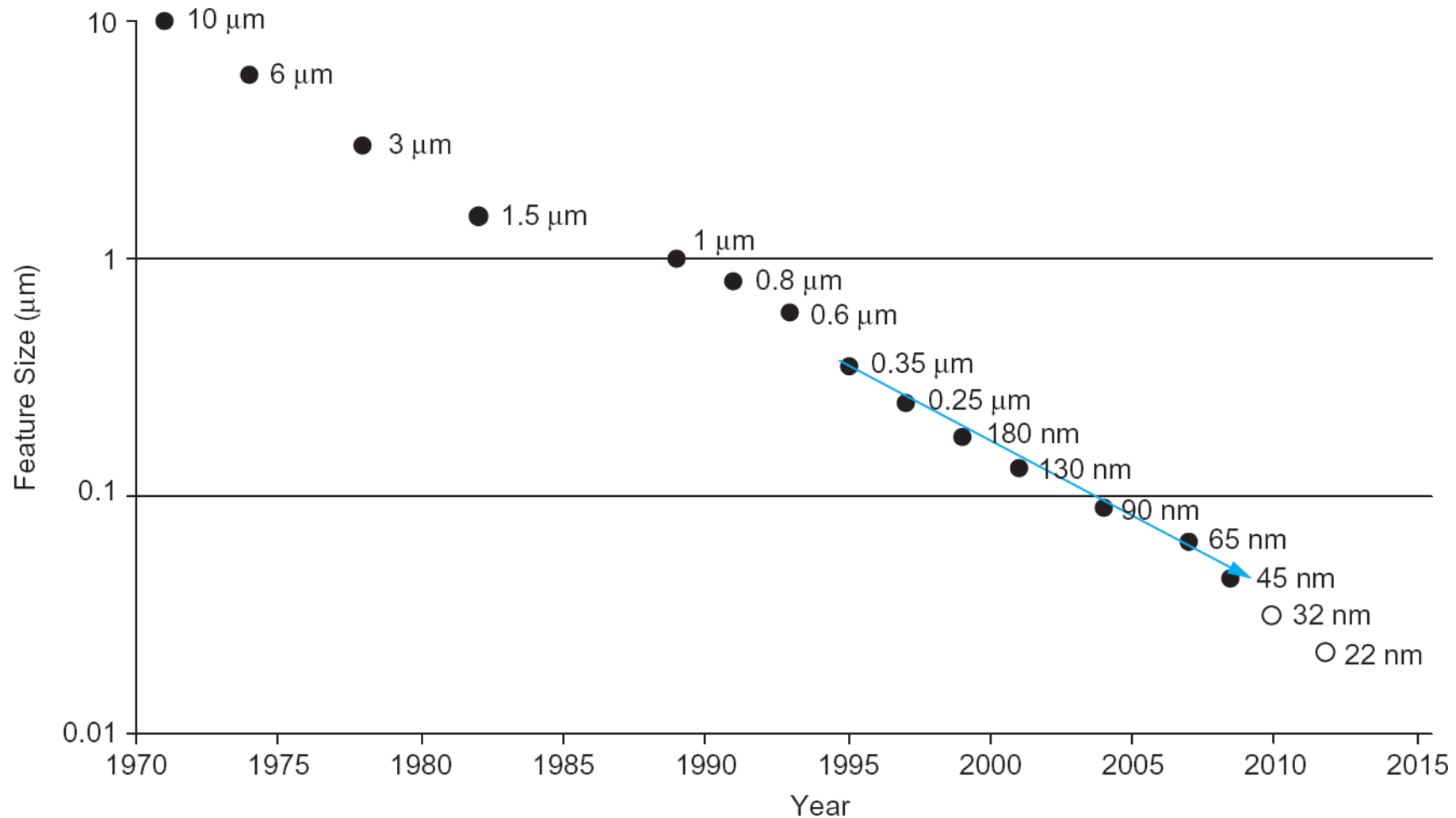
2020: Cerebras Systems AI Chip—1.2 Trillion Transistors!



Transistor Counts (Another Look)



Shrinking Transistor Sizes



Shrinking Transistor Sizes

FEBRUARY 20, 2020

Logic/Foundry Process Roadmaps (for Volume Production)

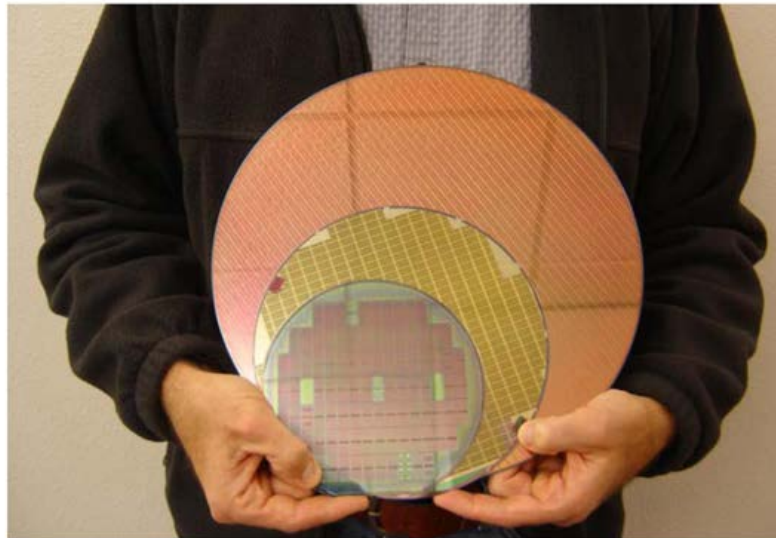
	2015	2016	2017	2018	2019	2020	2021
Intel		14nm+	10nm (limited) 14nm++		10nm	10nm+	7nm EUV 10nm++
Samsung	28nm FDSOI	10nm		8nm	7nm EUV 6nm EUV	18nm FDSOI 5nm	4nm
TSMC	16nm+ finFET	10nm	7nm 12nm		7nm+ EUV	5nm 6nm	5nm+
GlobalFoundries	14nm finFET			22nm FDSOI 12nm finFET		12nm FDSOI	12nm+ finFET
SMIC	28nm				14nm finFET	12nm finFET	
UMC			14nm finFET			22nm planar	

Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embellishments, so these points of transition should only be seen as very general guidelines.

Sources: Companies, conference reports, IC Insights

Wafer Sizes

- » Larger wafers allow more die to be produced in parallel:

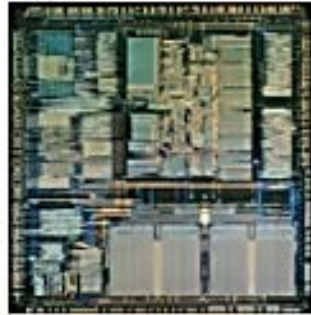


R. J. Baker, "CMOS: Circuit design, layout, and simulation," 2019.

- » Each die is identical

Intel Processors Over the Years

1985



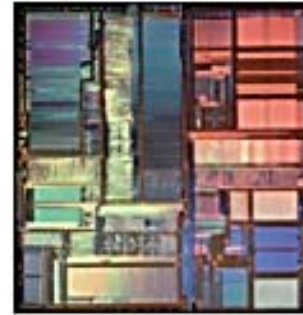
Intel 386[®] processor
Initial clock speed: 10MHz
Transistors: 275,000
Manufacturing technology: 1.5 micron

1989



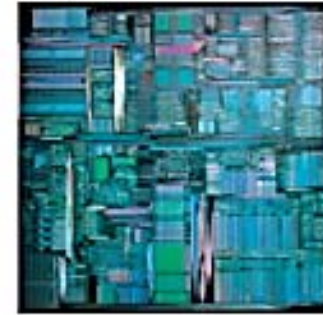
Intel 486[®] processor
Initial clock speed: 25MHz
Transistors: 1.2 million
Manufacturing technology: 1 micron

1993



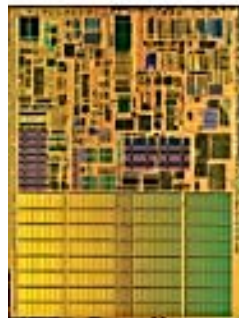
Intel[®] Pentium[®] processor
Initial clock speed: 66MHz
Transistors: 3.1 million
Manufacturing technology: 0.8 micron

1995



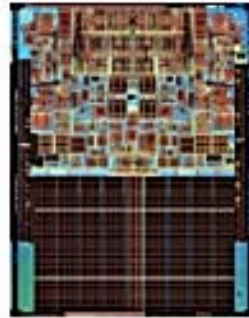
Intel[®] Pentium[®] Pro processor
Initial clock speed: 200MHz
Transistors: 5.5 million
Manufacturing technology: 0.35 micron

2003



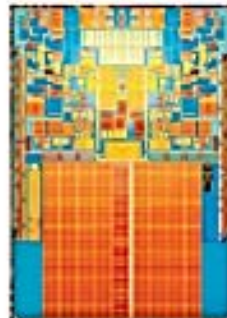
Intel[®] Pentium[®] M processor
Initial clock speed: 1.7GHz
Transistors: 55 million
Manufacturing technology: 90nm

2006



Intel[®] Core[™]2 Duo processor
Initial clock speed: 2.66GHz
Transistors: 291 million
Manufacturing technology: 65nm

2008



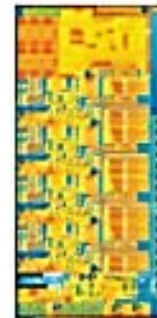
Intel[®] Core[™]2 Duo processor
Initial clock speed: 2.4GHz
Transistors: 410 million
Manufacturing technology: 45nm

2008



Intel[®] Atom[™] processor
Initial clock speed: 1.86GHz
Transistors: 47 million
Manufacturing technology: 45nm

2010



2nd generation Intel[®] Core[™] processor
Initial clock speed: 3.8GHz
Transistors: 1.16 billion
Manufacturing technology: 32nm

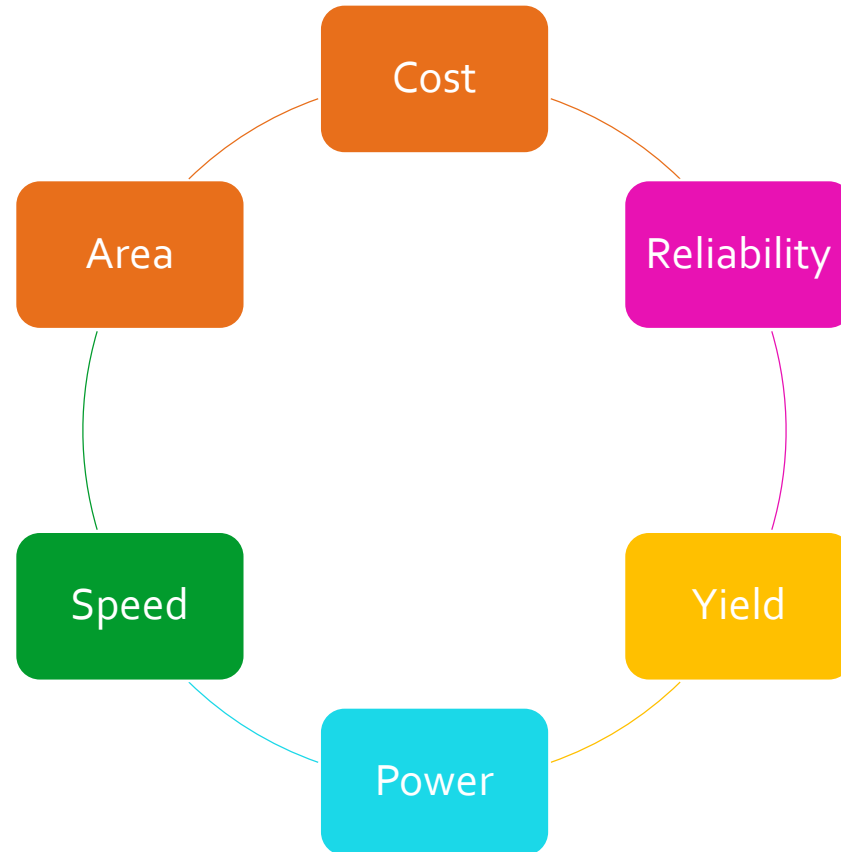
2012



3rd generation Intel[®] Core[™] processor
Initial clock speed: 2.9GHz
Transistors: 1.4 billion
Manufacturing technology: 22nm

Evaluating Digital ICs

- » What are the tradeoffs?
- » What influences what?



Shrinking Transistor Sizes

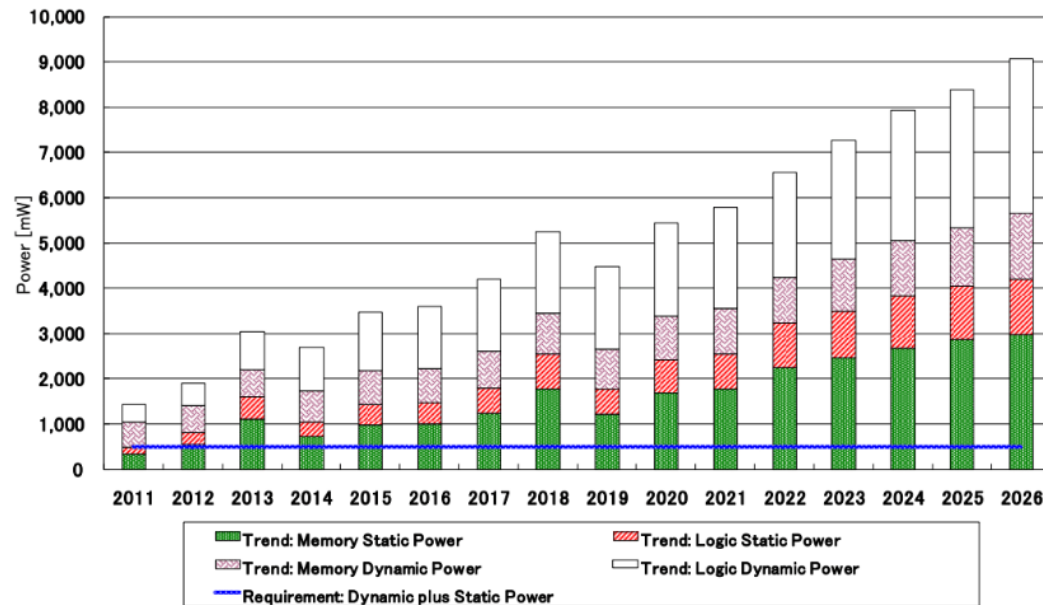
» Why does the IC industry want to scale?

Parameter	Sensitivity	Dennard Scaling	Constant Voltage	Lateral Scaling
L: Length		1/S	1/S	1/S
W: Width		1/S	1/S	1
t_{ox} : gate oxide thickness		1/S	1/S	1
V_{DD} : supply voltage		1/S	1	1
V_t : threshold voltage		1/S	1	1
NA: substrate doping		S	S	1
β	$W/(Lt_{ox})$	S	S	S
I_{on} : ON current	$\beta(V_{DD}-V_t)^2$	1/S	S	S
R: effective resistance	V_{DD}/I_{on}	1	1/S	1/S
C: gate capacitance	WL/t_{ox}	1/S	1/S	1/S
τ : gate delay	RC	1/S	$1/S^2$	$1/S^2$
f: clock frequency	$1/\tau$	S	S^2	S^2
E: switching energy / gate	CV_{DD}^2	$1/S^3$	1/S	1/S
P: switching power / gate	Ef	$1/S^2$	S	S
A: area per gate	WL	$1/S^2$	$1/S^2$	1
Switching power density	P/A	1	S^3	S
Switching current density	I_{on}/A	S	S^3	S

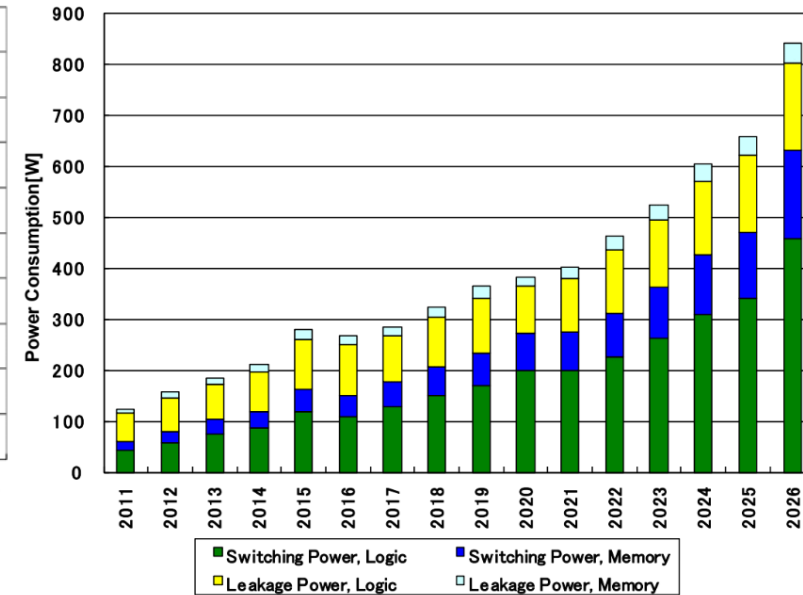
Faster, more energy-efficient chips @ lower cost

Adverse Effects of Scaling

» Power Consumption



Source: ITRS

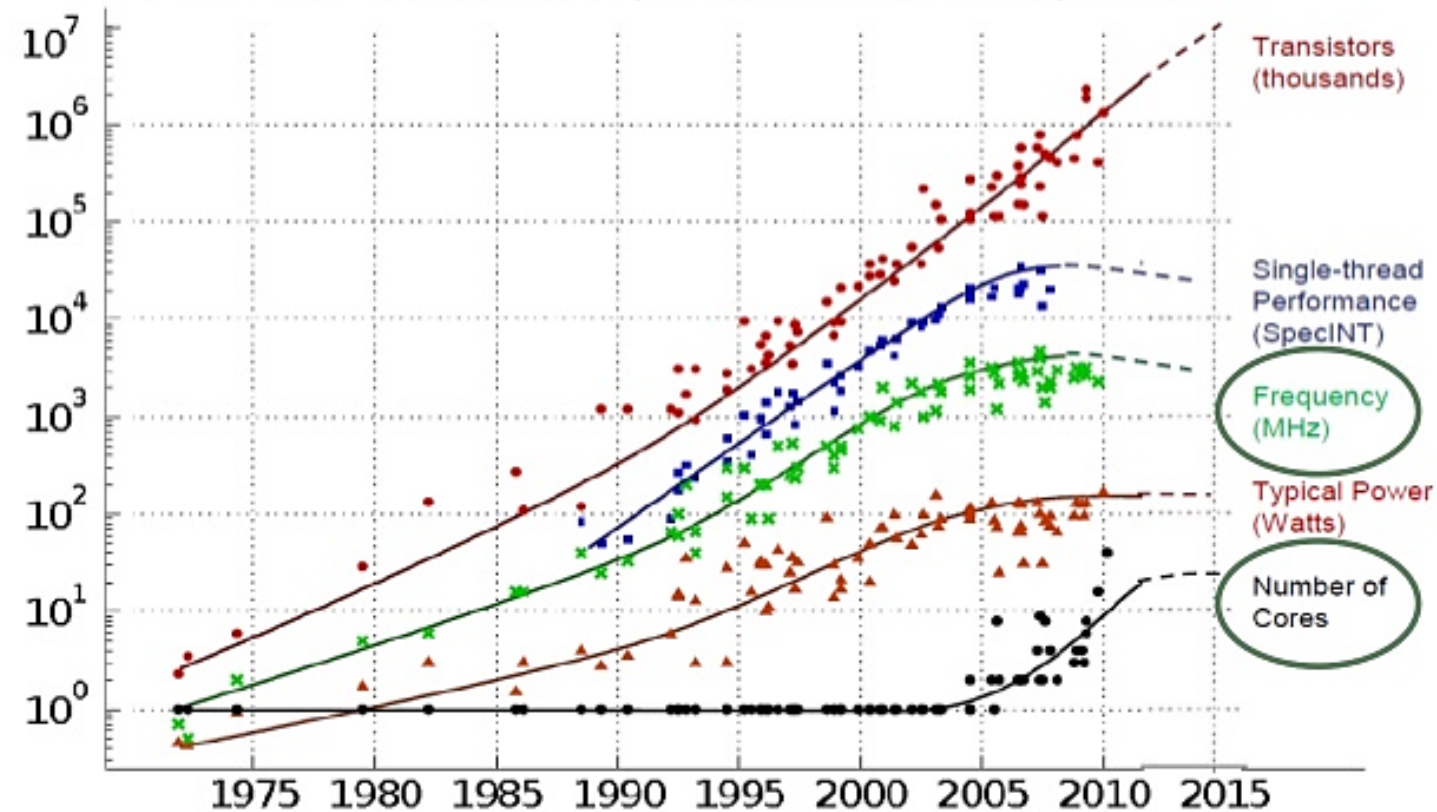


- » More transistors/chip → More dynamic power
- » As threshold voltages are reduced, transistors become more “leaky”
 - Large static power consumption



The Death of Moore's Law ☹️

Power and Heat Problems Led to Multiple Cores and Prevent Further Improvements in Speed



Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

Source: Chuck Moore, Data Processing in Exascale-Class Systems, April 27, 2011. Salishan Conference on High Speed Computing

The Different Ages of Scaling

(Different methods for different times)

1 Geometrical Scaling (1975-2002)

- ◆ Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors

2 Equivalent Scaling (2003~2024)

- ◆ Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor

3 3D Power Scaling (2025~2040)

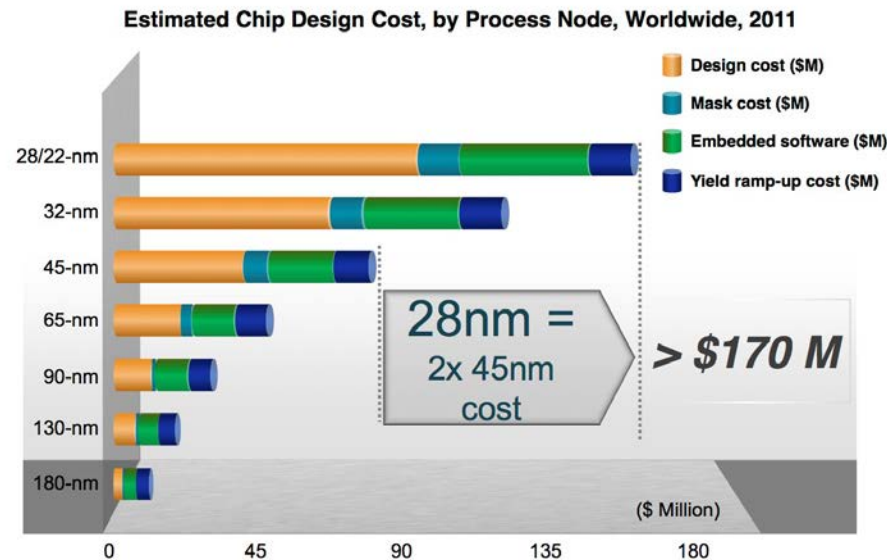
- ◆ Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers



Adverse Effects of Scaling

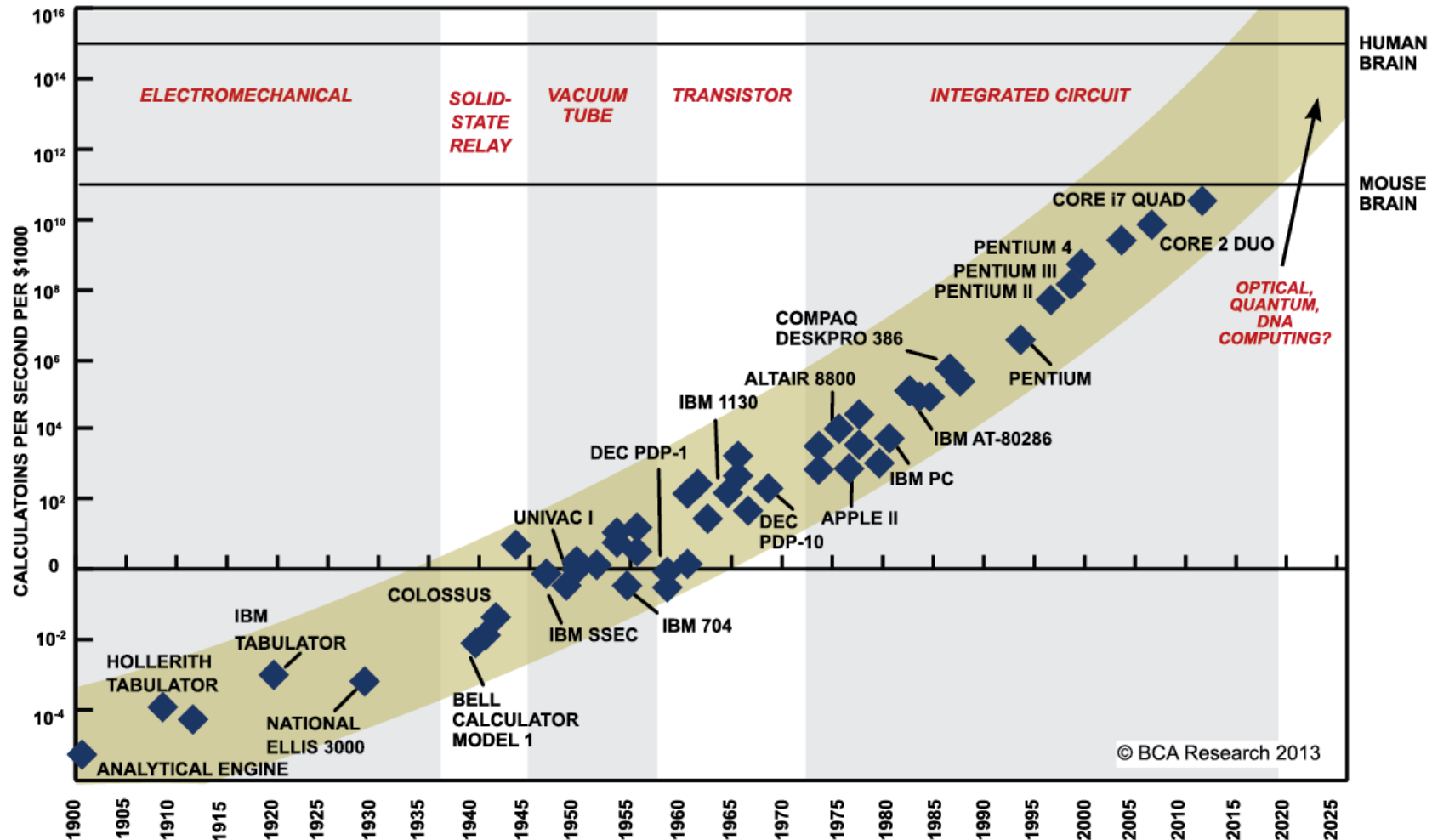
- » Reliability
- » Design/manufacturing cost
 - Barrier to entry for new businesses
 - SOC design cost approaching \$500M

Design Cost



Source: Xilinx

Another View of Moore's Law



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, THE VIKING PRESS, 2006. DATAPPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Another View of Moore's Law

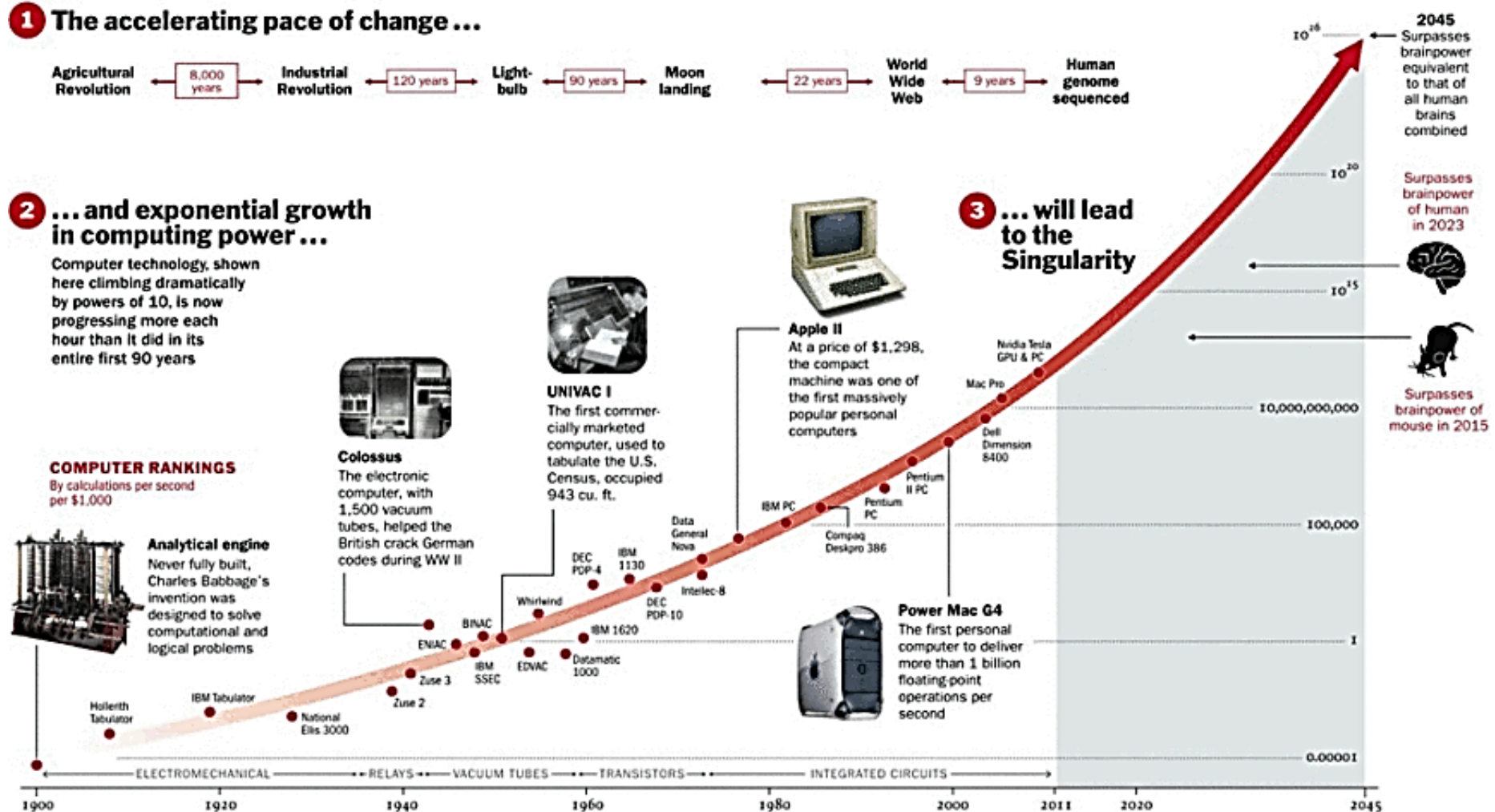
1 The accelerating pace of change ...



2 ... and exponential growth in computing power ...

Computer technology, shown here climbing dramatically by powers of 10, is now progressing more each hour than it did in its entire first 90 years.

3 ... will lead to the Singularity



Back to Our 1-bit Multiplier Example

» There are lots of approaches we could use:

- Full Custom
 - Every gate is custom designed
 - Most flexible for efficiency
 - Too difficult these days with billions of gates
- Application Specific Integrated Circuit
 - Gates come from a library, most effort goes into floorplanning, routing
- System-on-Chip (SOC)
 - Many heterogeneous functionalities on one die
 - Analog/digital/RF, etc.
- System-in-Package (SIP)
 - Several dice integrated into one package

Additional Reading

- » International Technology Roadmap for Semiconductors (ITRS)
 - www.itrs2.net/
- » International Roadmap for Devices and Systems
 - <https://irds.ieee.org/>
- » Moore, G. E. (1998). Cramming more components onto integrated circuits. *Proceedings of the IEEE*, 86(1), 82-85.
- » Feynman, R. P. (2012). There's plenty of room at the bottom: An invitation to enter a new field of physics. In *Handbook of Nanoscience, Engineering, and Technology, Third Edition* (pp. 26-35). CRC Press.
- » *Crystal Fire* by Michael Riordan and Lillian Hoddeson
- » *The Chip* by T. R. Reid
- » <http://www.computerhistory.org/timeline>