Digital Integrated Circuit Design

CMPE 530/630

IC Fabrication and Layout

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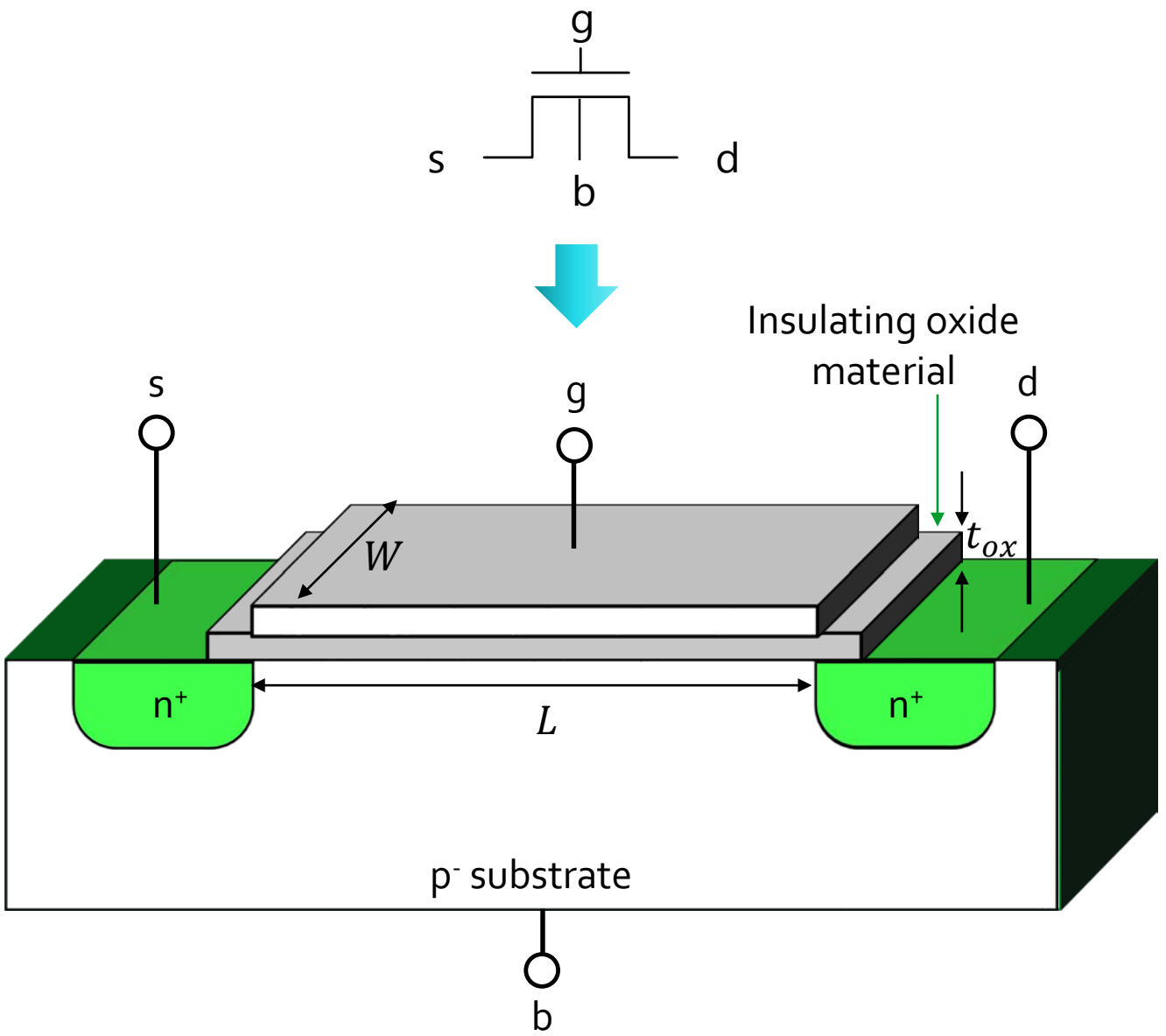
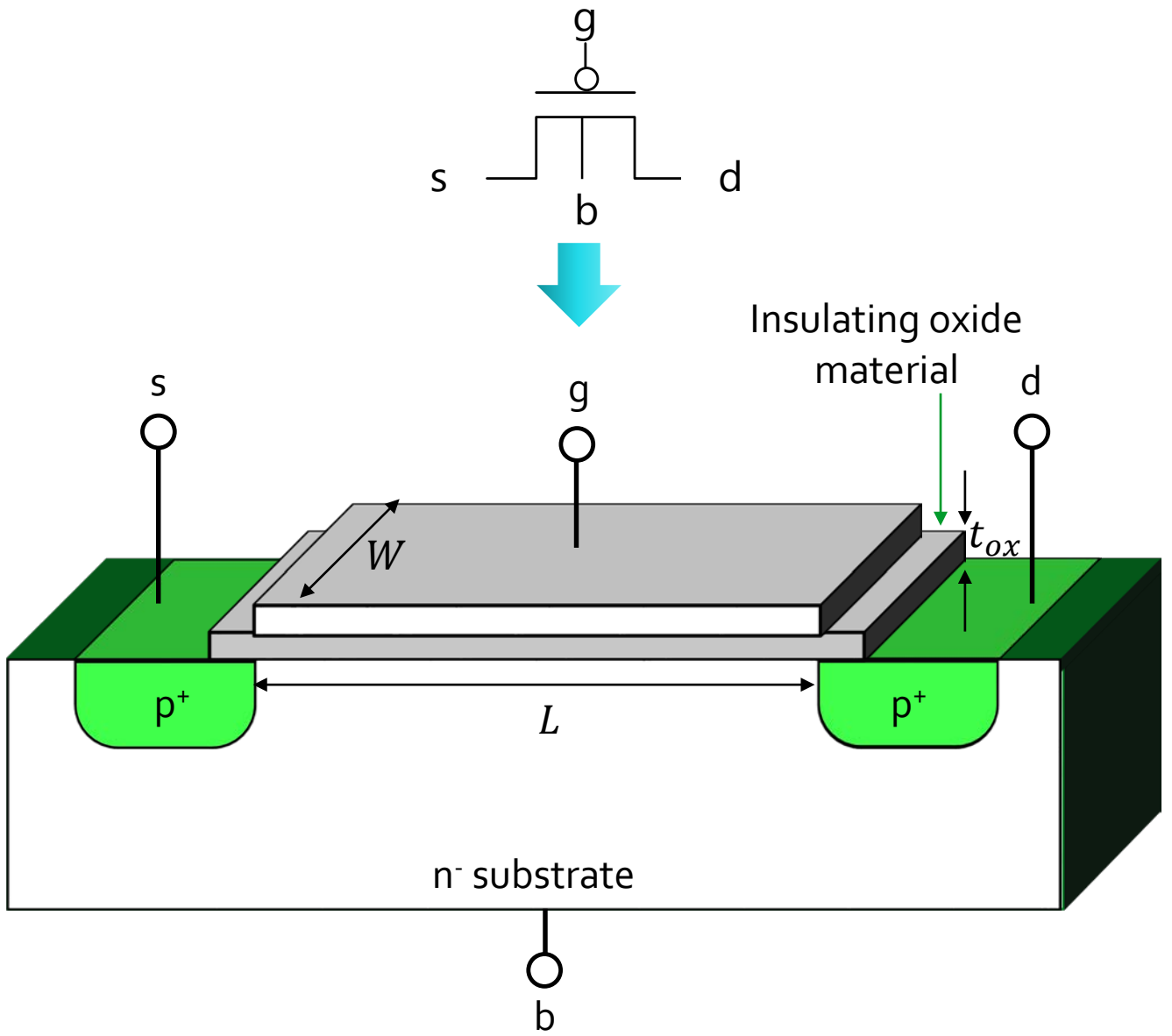
Learning Objectives

- Understand the basic process of fabrication CMOS ICs
- Be able to draw a stick diagram from a CMOS circuit using the Euler's path technique
- Be able to design a mask set for a CMOS circuit that follows a given set of lambda rules

Physical Realization of nMOSFET

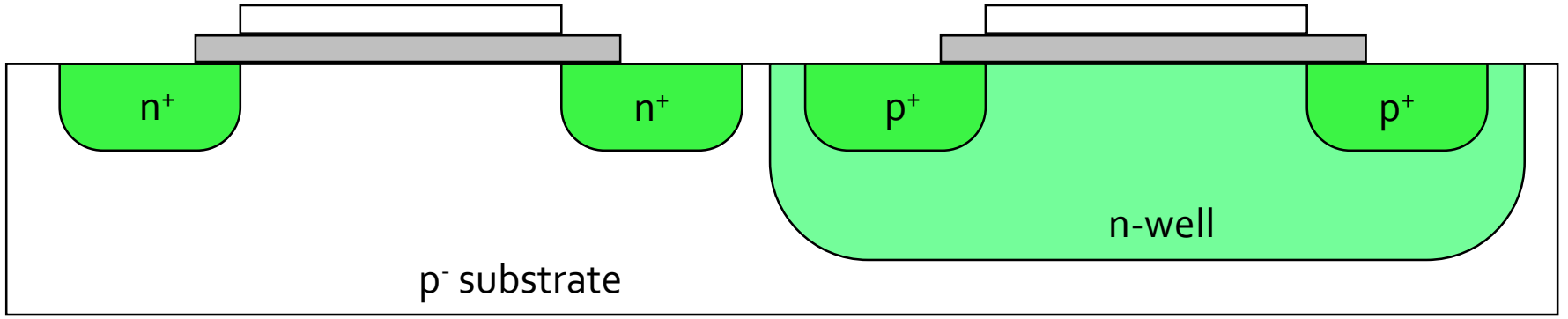


Physical Realization of pMOSFET



NMOS and PMOS Together

» In an *n-well process*, n-type dopants are diffused into the silicon to form a well that acts as the PMOS substrate:



» We always connect NMOS bodies to ground and PMOS bodies to V_{dd} to avoid current flowing through the substrate

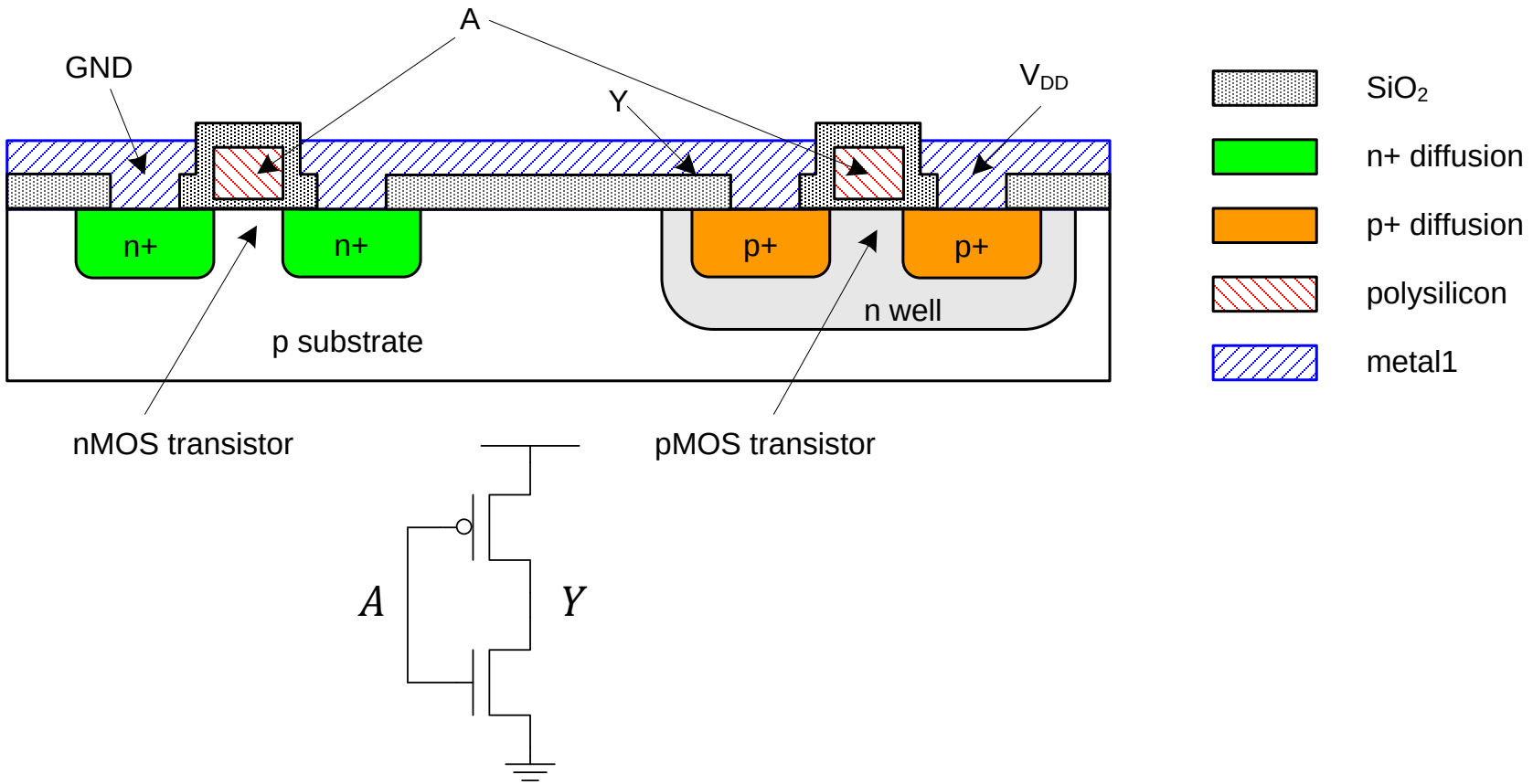
- We want all of the p-n junctions to be reverse-biased

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

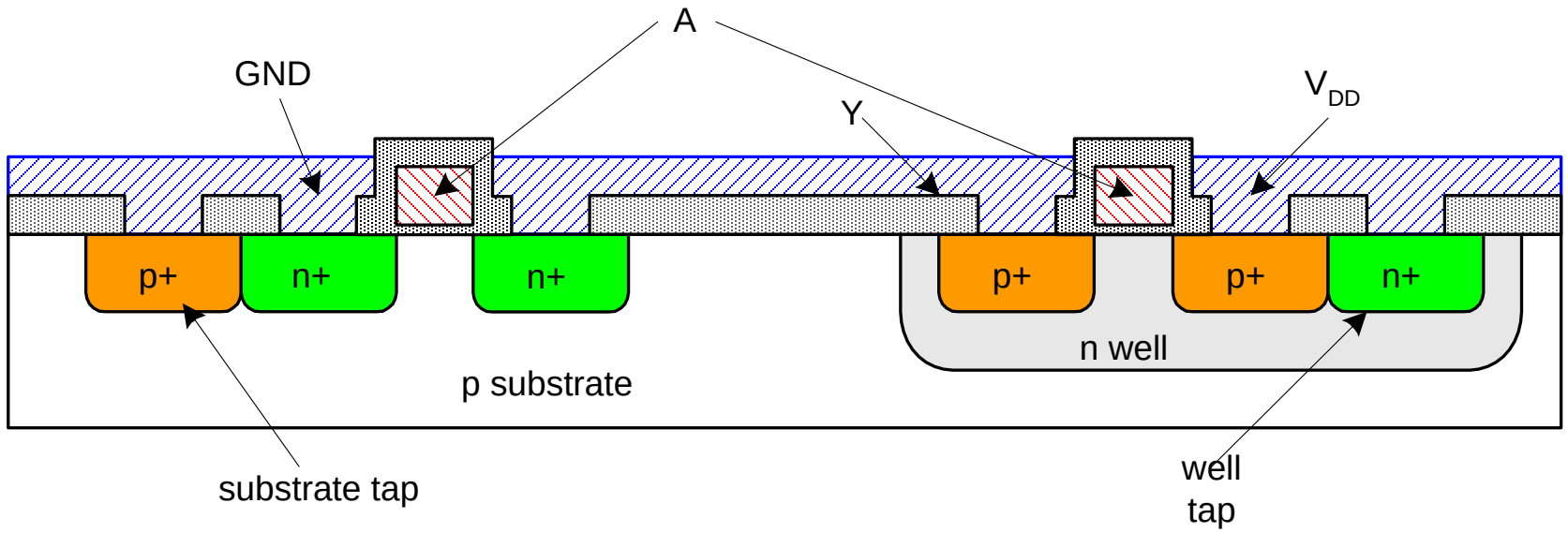
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



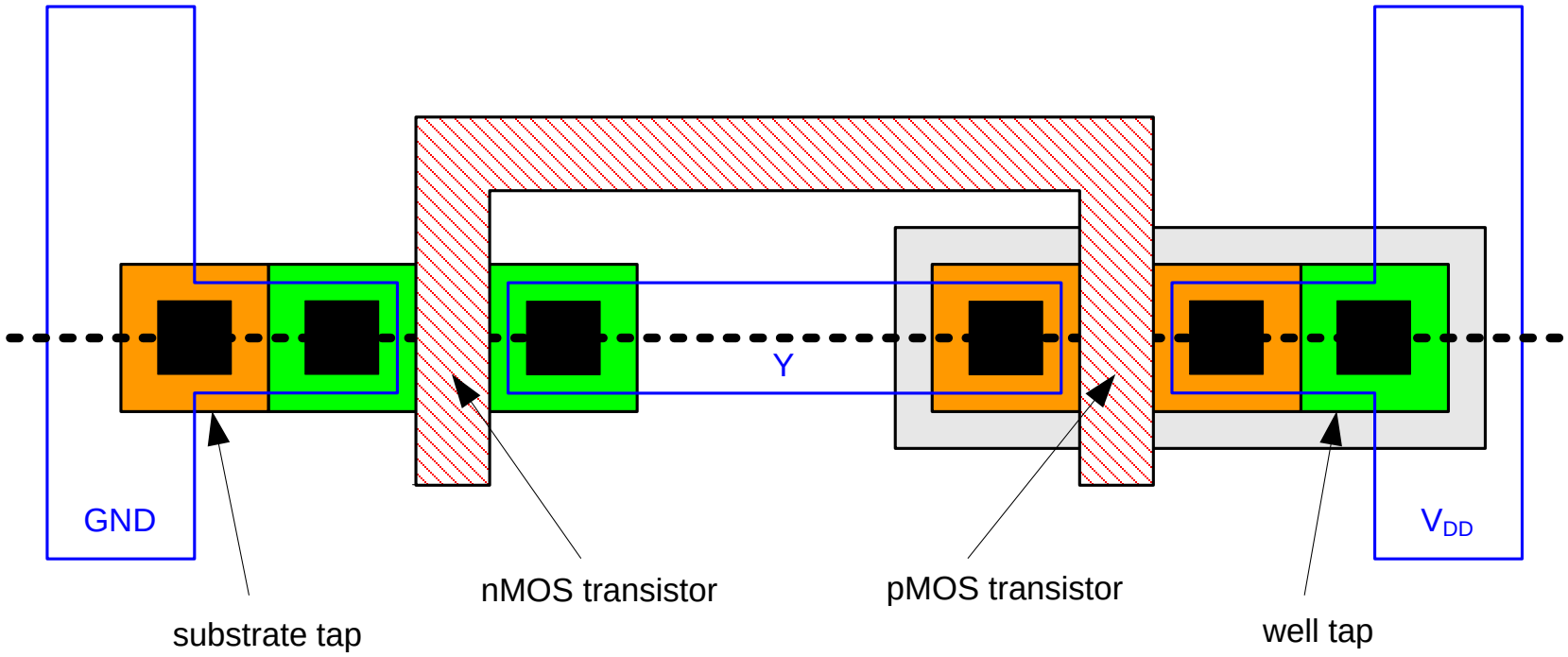
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



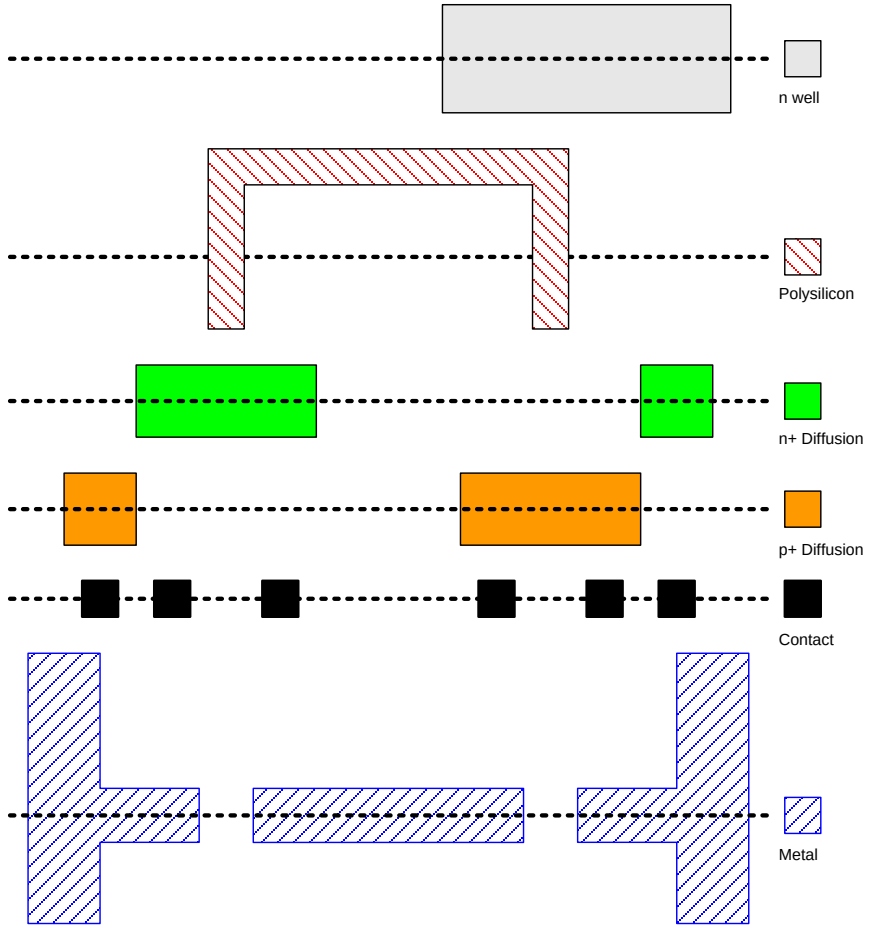
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
- Modern processes can have 60 or more masks

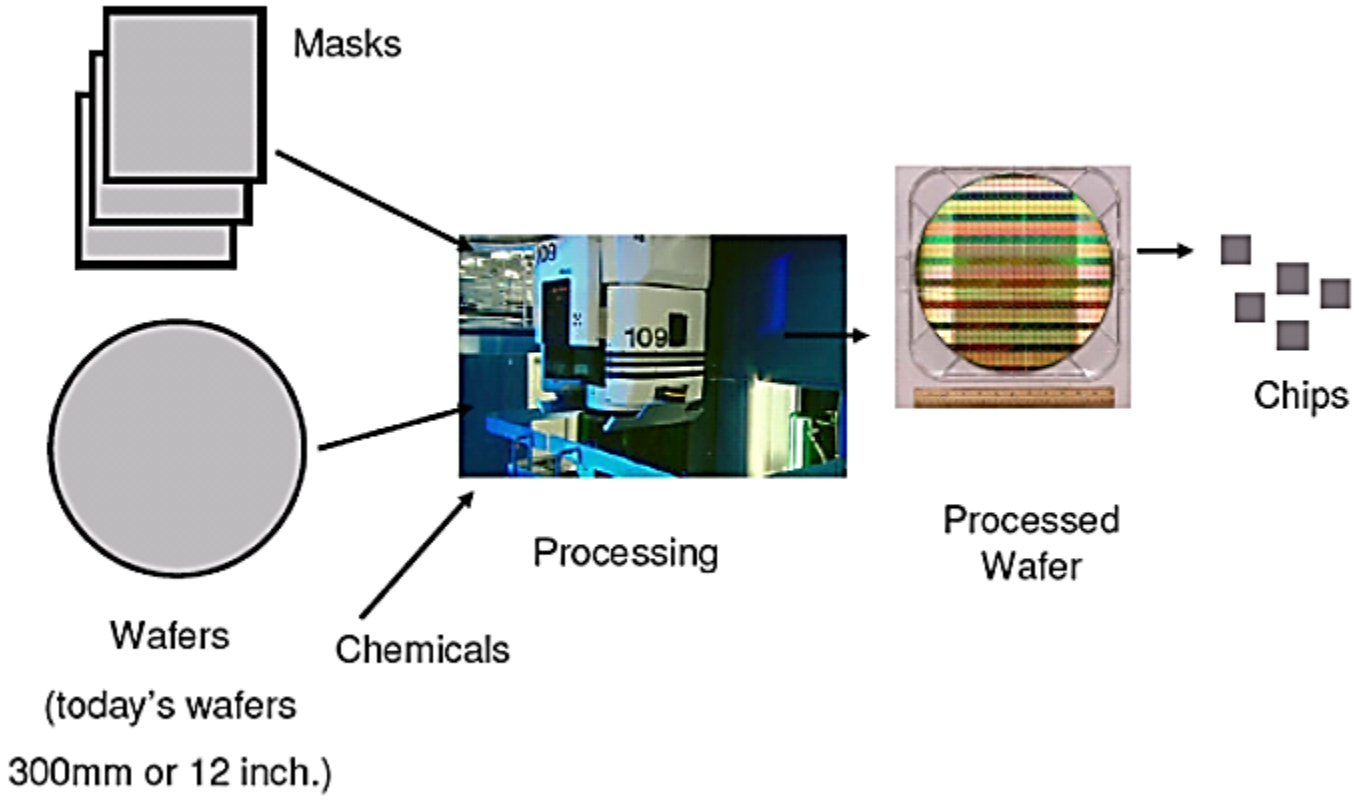


Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

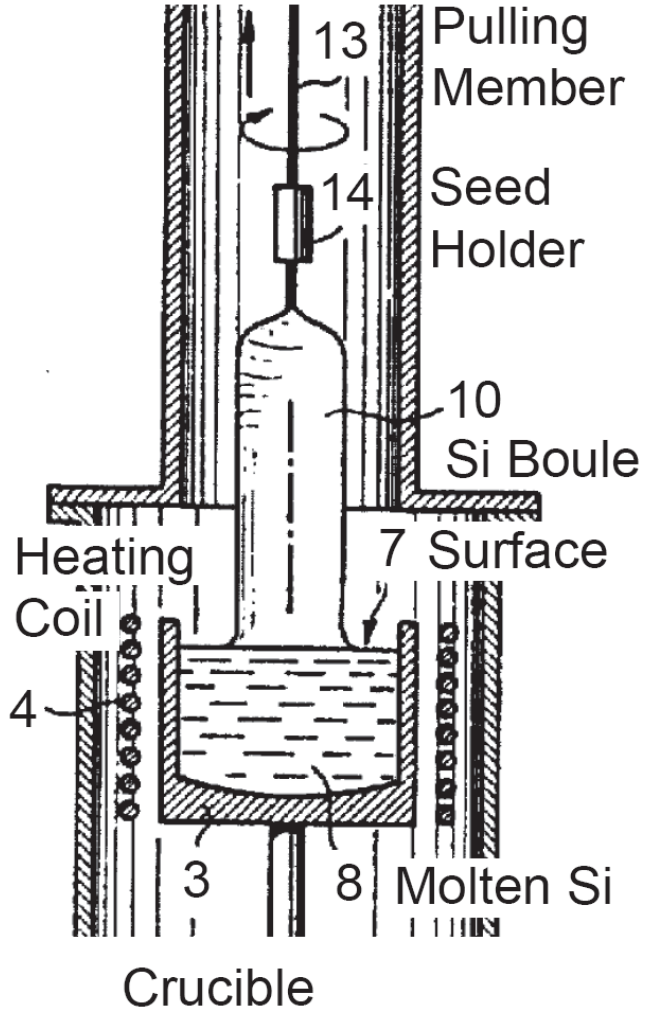
Modern fabs cost > $15b!

Basic Fabrication Flow



Making Silicon Wafers

- Czochralski process:
  - Si boules are grown by dipping a "seed" into molten Si and slowly pulling up and rotating
  - As boule is pulled up, it cools and crystallizes
  - Speed of pulling/rotating determines diameter of boule
    - 300 mm is standard
- Boules are sliced into wafers less than 1mm thick
- Dopants added for p/n type Si

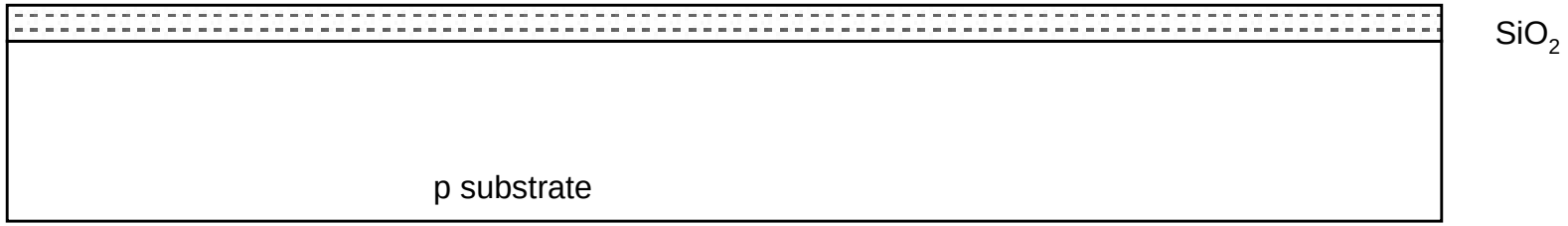


Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



Photoresist

» Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light

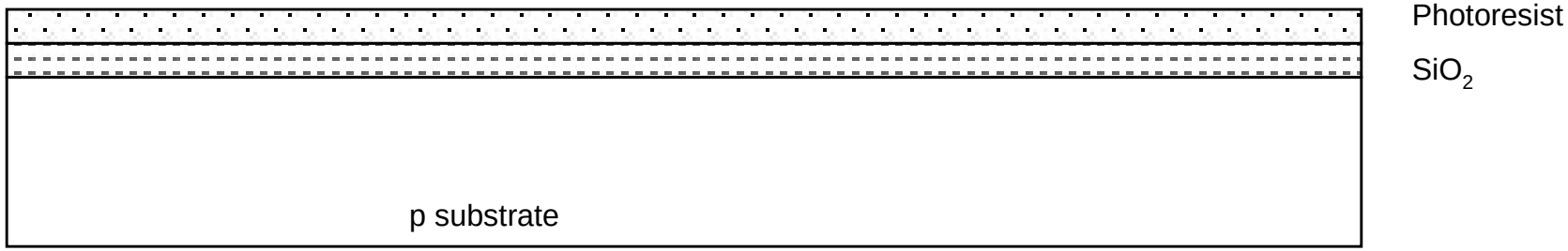
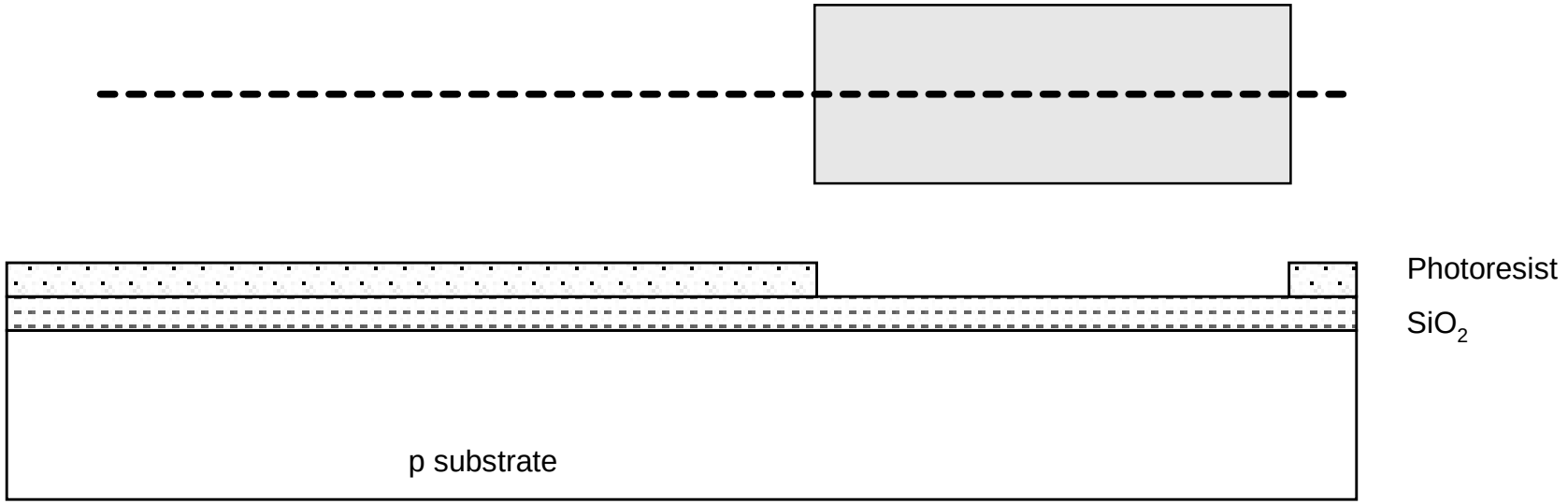


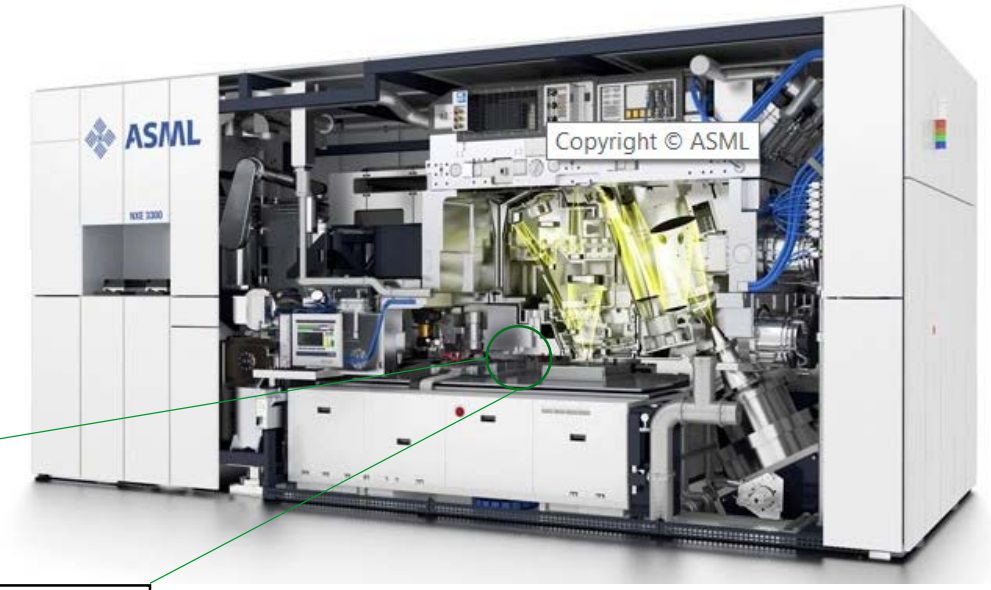
Photo Lithography

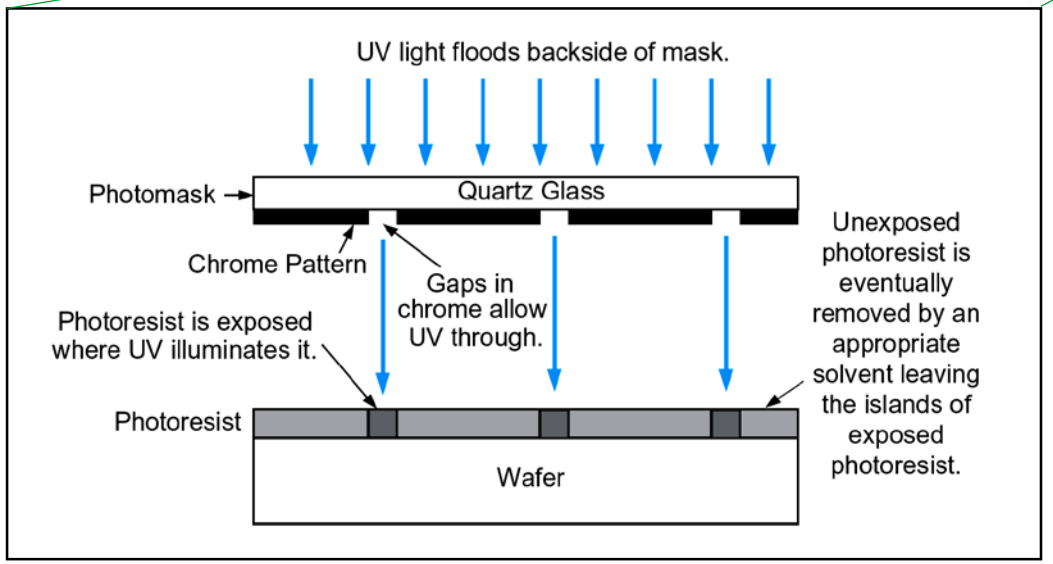
- Expose photoresist through n-well mask
- Strip off exposed photoresist



Photolithography

» Large machines called steppers are used to project light onto the wafer through the mask at extremely high resolution

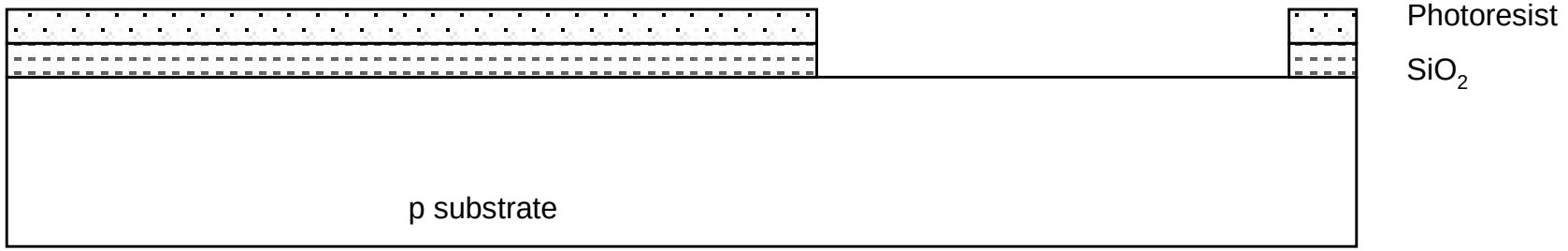




Source: www.zeiss.com

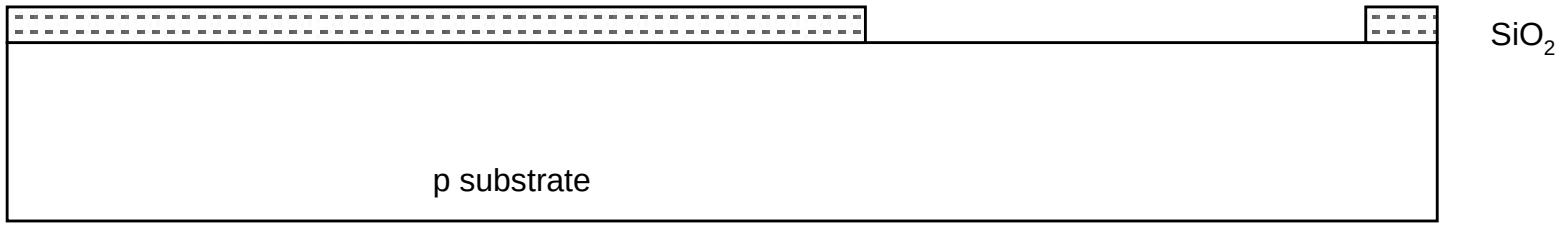
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



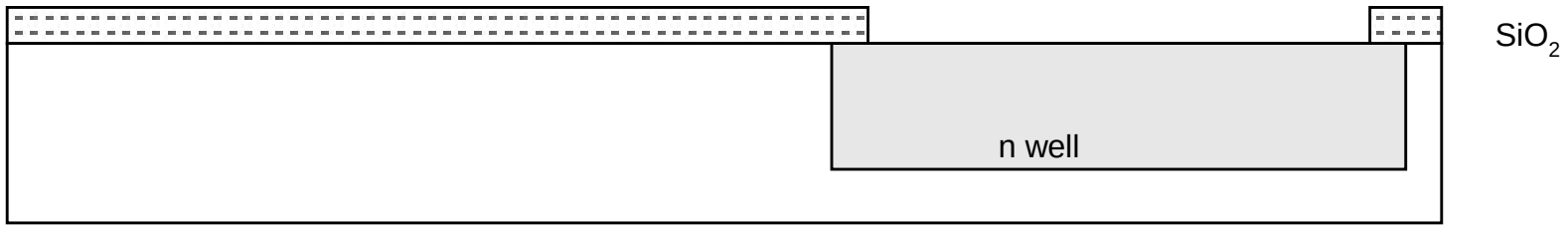
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



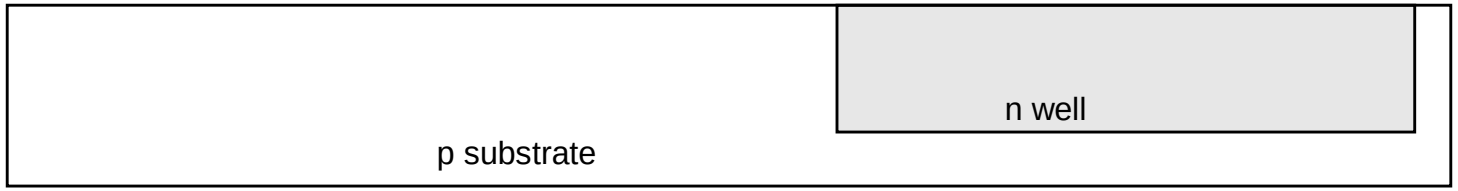
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



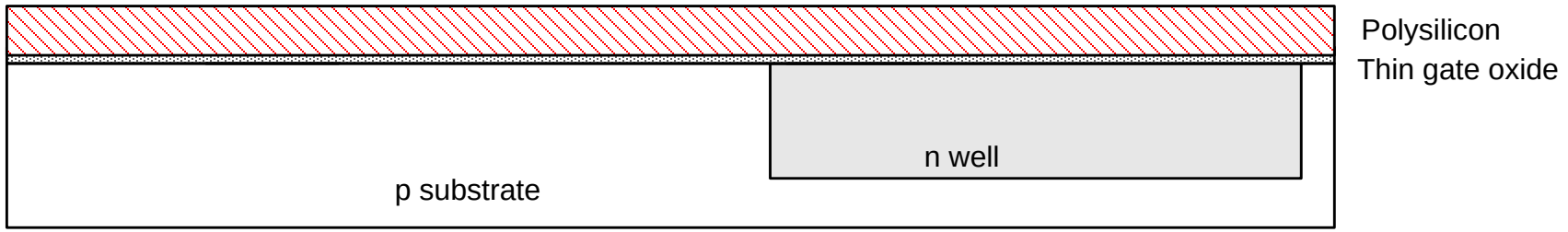
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



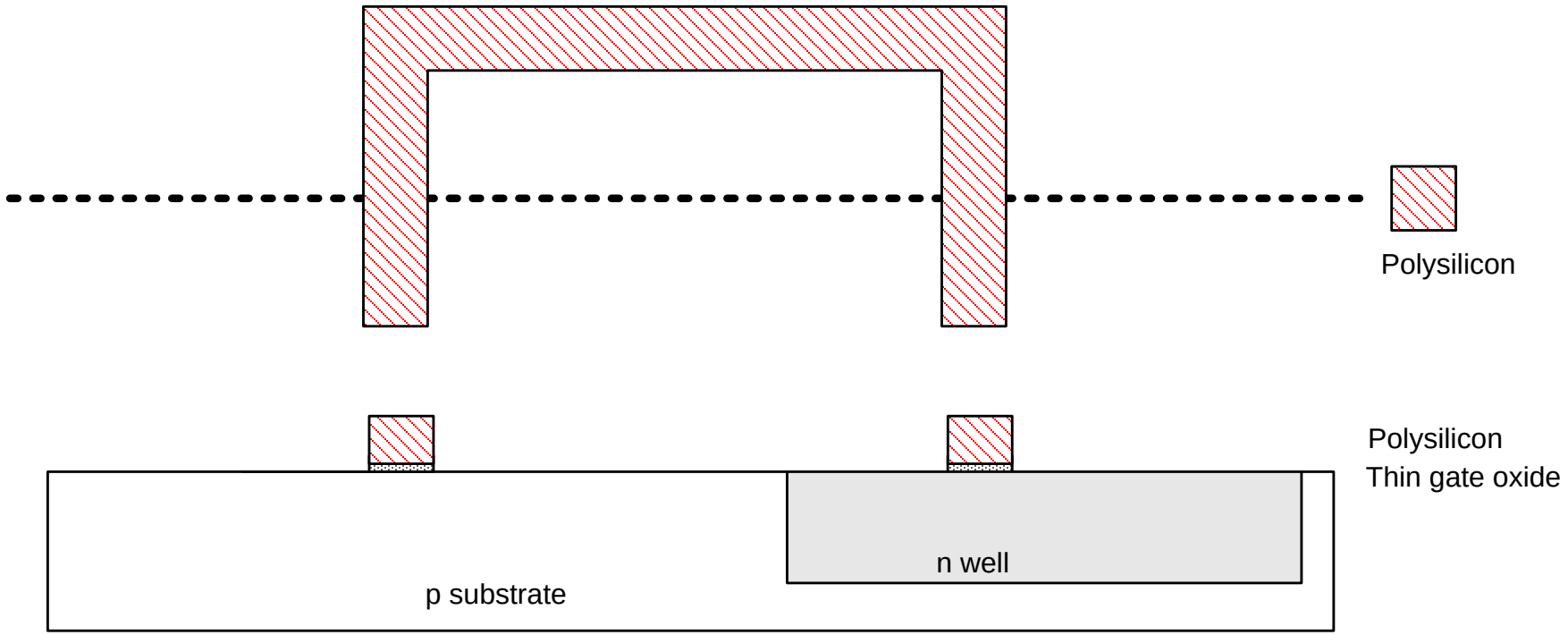
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



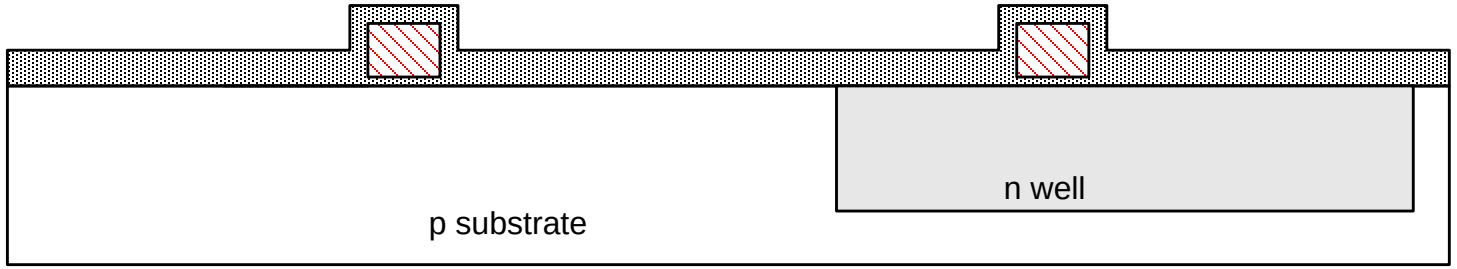
Polysilicon Patterning

» Use same lithography process to pattern polysilicon



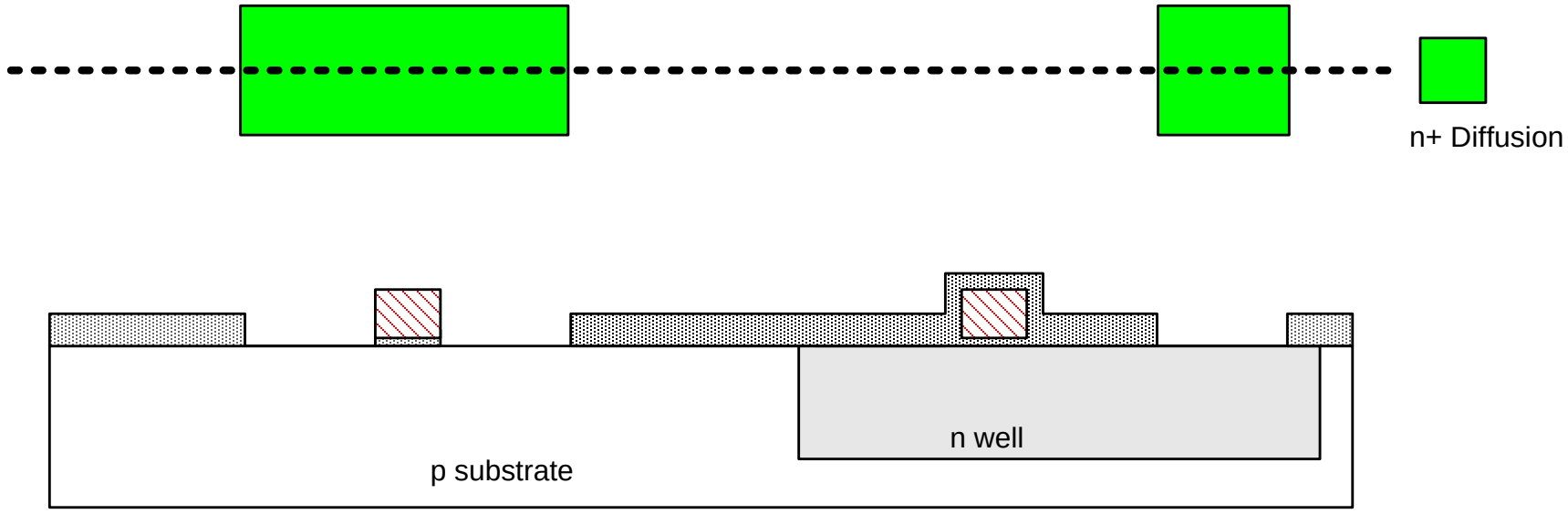
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



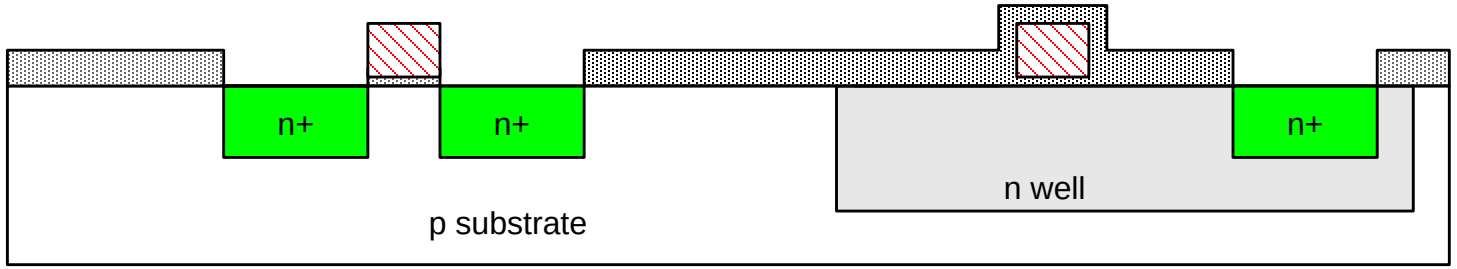
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



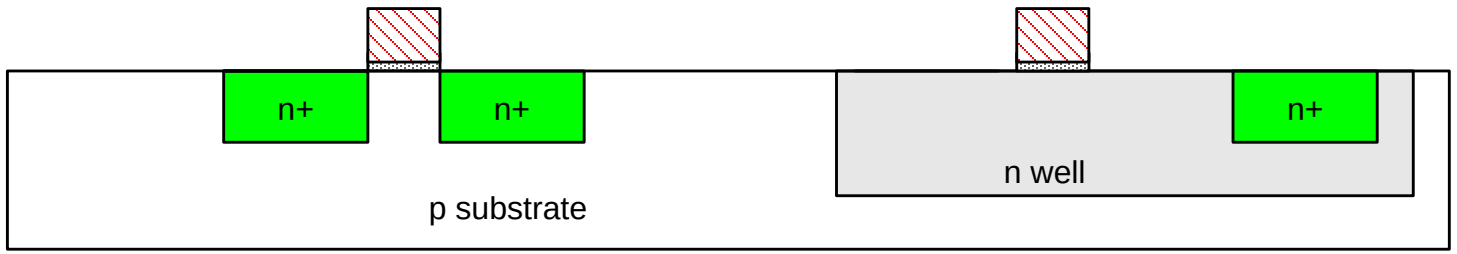
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



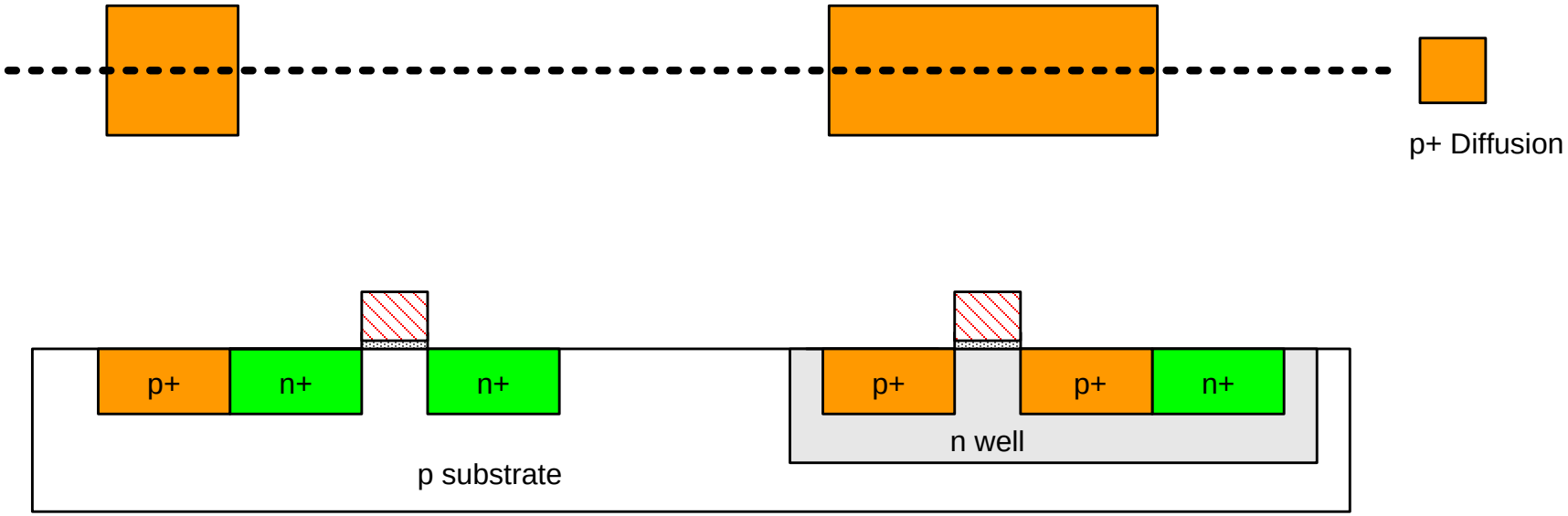
N-diffusion cont.

» Strip off oxide to complete patterning step



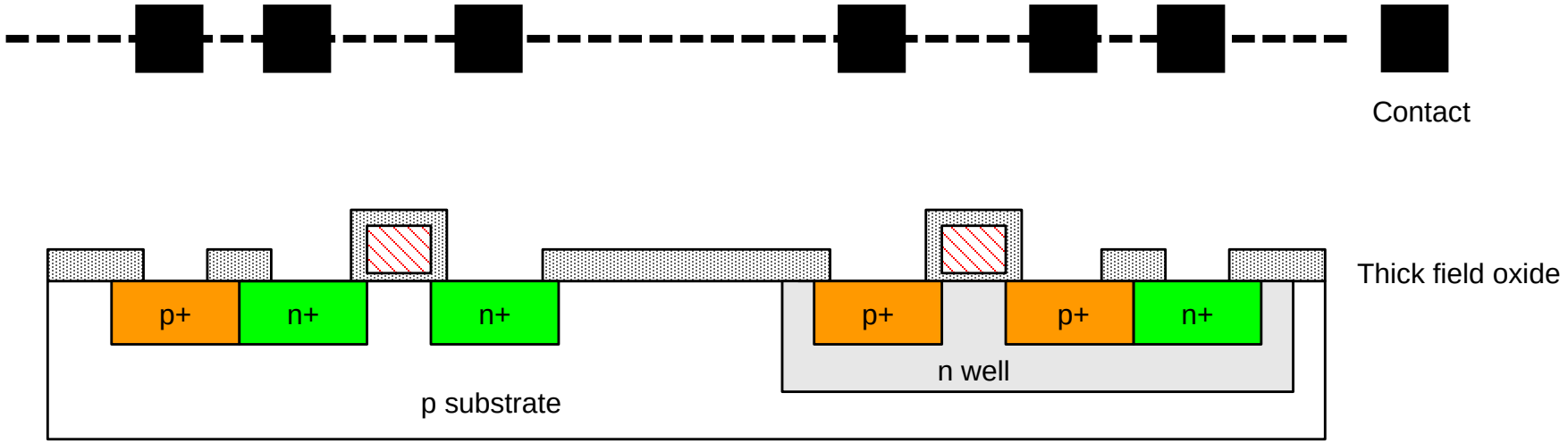
P-Diffusion

» Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



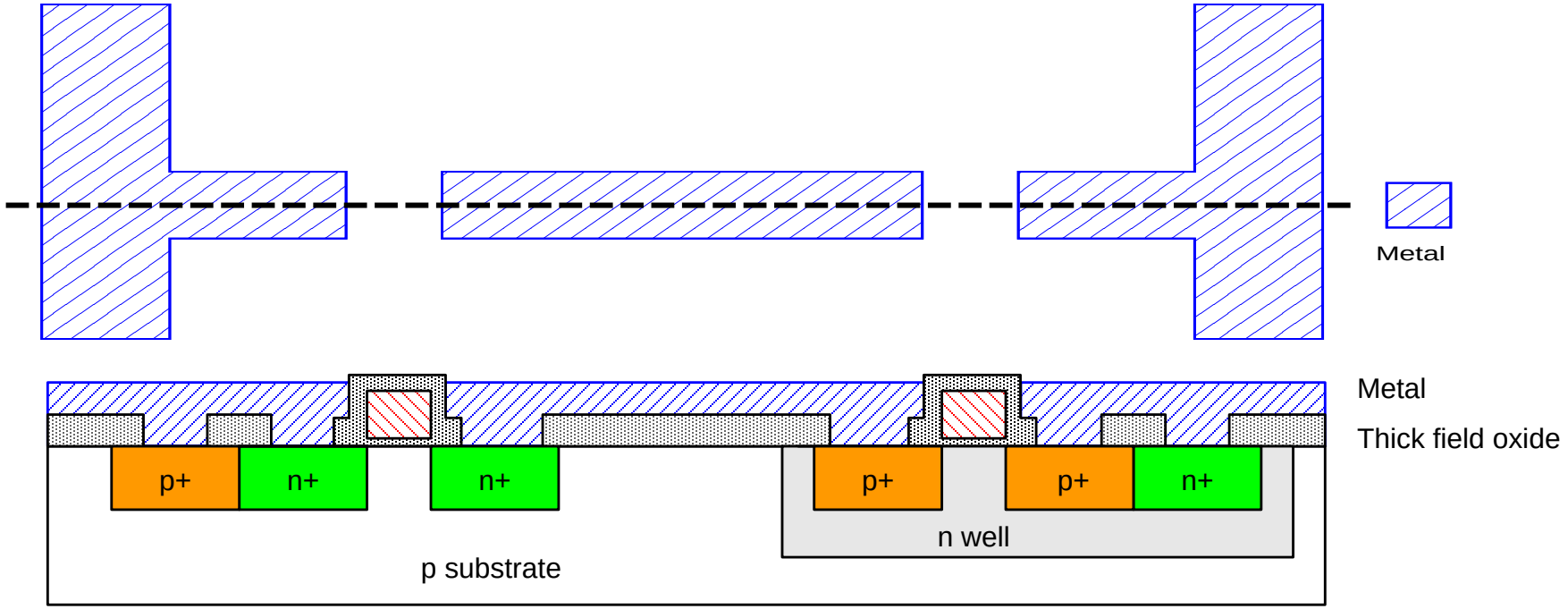
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

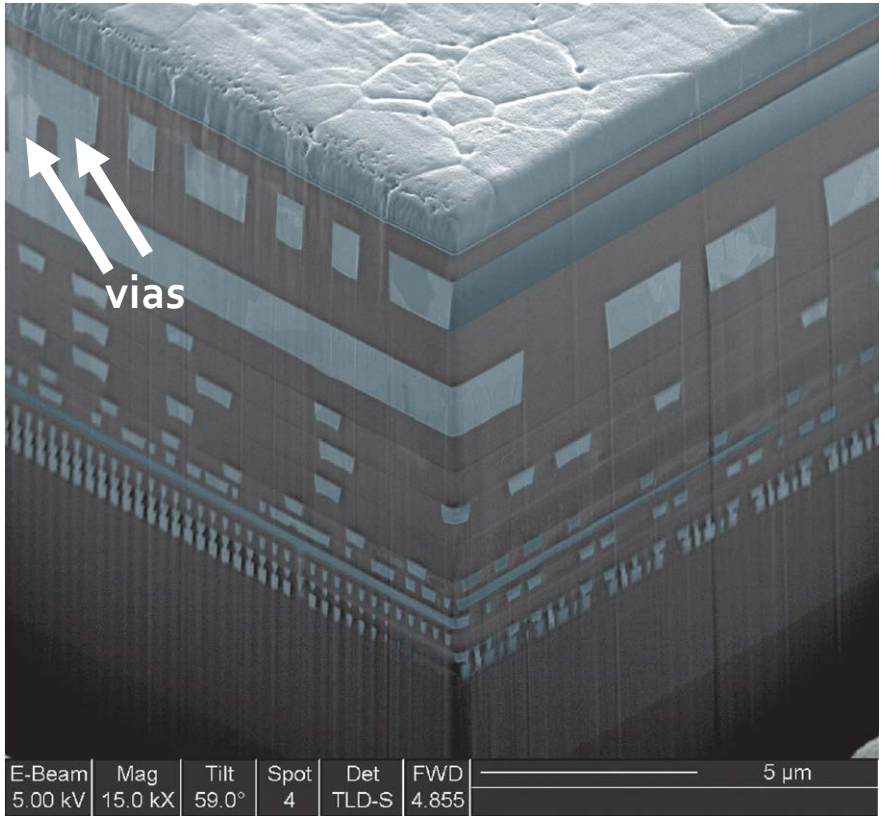
- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires
- Contacts between metal layers are called vias



Metallization

- 11 layers of metallization in an IBM process:

- Modern processes contain even more
  - Sometimes we even stack chips on top of each other!



Design Rules

- Motivation
  - Provide tradeoff between robustness/yield and performance/area

- 3 Types:
  - Minimum width
  - Minimum overlap
  - Minimum separation

- Become very complex as technology nodes shrink

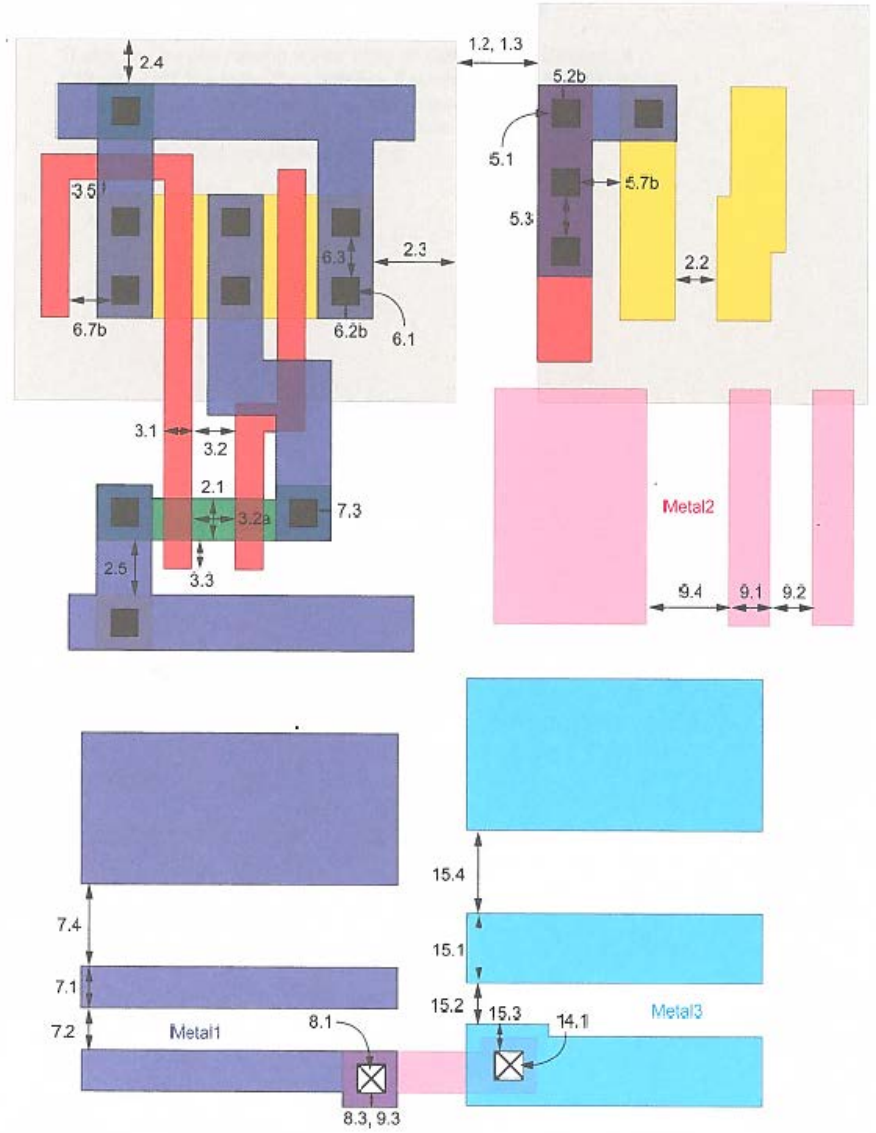
Types of Design Rules

- Absolute (e.g. micron rules)
  - Give the best optimization opportunities
  - Not scalable (have to change layout for each new technology node)

- Lambda-based (e.g. Scalable CMOS)
  - Layout doesn't need to change for new technology node
  - Specified as multiples of λ, which is usually half the minimum drawn channel length ($L = 2\lambda$)
  - MOSIS no longer supports SCMOS rules on anything but ON Semiconductor 0.5 μ technology

SCMOS Design Rules

MOSIS SUBM design rules (3 metal, 1 poly with stacked vias & alternate contact rules)			
Layer	**Rule**	**Description**	**Rule (λ)**
N-well	1.1	Width	12
	1.2	Spacing to well at different potential	18
	1.3	Spacing to well at same potential	6
Active (diffusion)	2.1	Width	3
	2.2	Spacing to active	3
	2.3	Source/drain surround by well	6
	2.4	Substrate/well contact surround by well	3
	2.5	Spacing to active of opposite type	4
Poly	3.1	Width	2
	3.2	Spacing to poly over field oxide	3
	3.2a	Spacing to poly over active	3
	3.3	Gate extension beyond active	2
	3.4	Active extension beyond poly	3
	3.5	Spacing of poly to active	1
Select (n or p)	4.1	Spacing from substrate/well contact to gate	3
	4.2	Overlap of active	2
	4.3	Overlap of substrate/well contact	1
	4.4	Spacing to select	2
Contact (to poly or active)	5.1, 6.1	Width (exact)	2×2
	5.2b, 6.2b	Overlap by poly or active	1
	5.3, 6.3	Spacing to contact	3
	5.4, 6.4	Spacing to gate	2
	5.5b	Spacing of poly contact to other poly	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/active contacts	3
	6.8b	Spacing of active contact to poly contact	4
Metal1, Metal2	7.1, 9.1	Width	3
	7.2, 9.2	Spacing to same layer of metal	3
	7.3, 8.3, 9.3	Overlap of contact or via	1
	7.4, 9.4	Spacing to metal for lines wider than 10λ	6
Via1, Via2	8.1, 14.1	Width (exact)	2×2
	8.2, 14.2	Spacing to via on same layer	3
Metal3	15.1	Width	5
	15.2	Spacing to metal3	3
	15.3	Overlap of via2	2
	15.4	Spacing to metal for lines wider than 10 λ	6
Overglass Cut	10.1	Width of bond pad opening	60 μm
	10.2	Width of probe pad opening	20 μm
	10.3	Metal3 overlap of overglass cut	6 μm
	10.4	Spacing of pad metal to unrelated metal	30 μm
	10.5	Spacing of pad metal to active or poly	15 μm

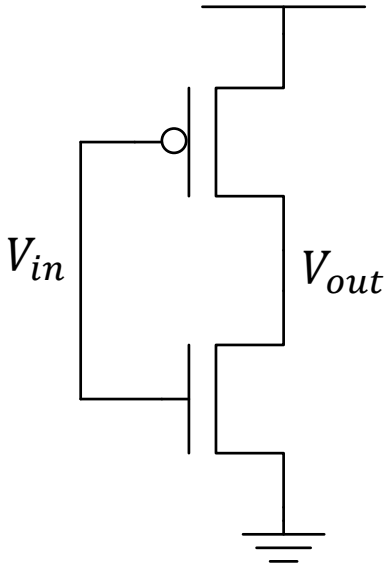


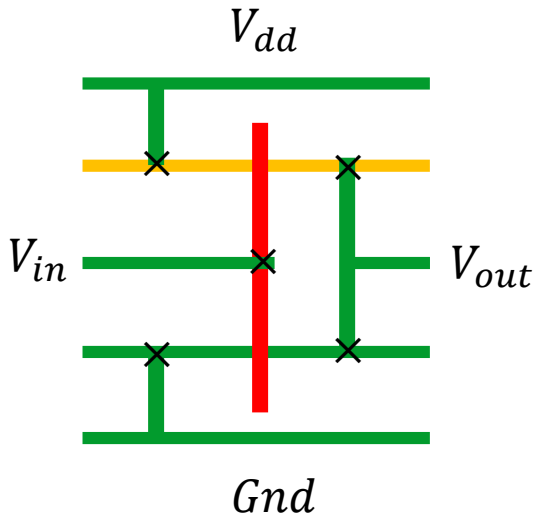
MOSIS Design Rules

Stick Diagrams

» Easy way to sketch mask designs

» Example: CMOS Inverter





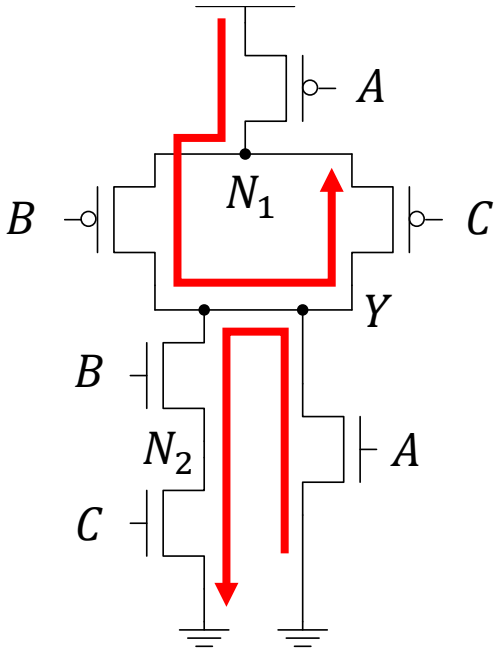
Metal 1
p+ diffusion
n+ diffusion
poly
× Contact

Euler's Path

- Euler's path helps us find a good order of the gates in our stick diagram/layout
- Find a path through the pull-up network that visits each transistor **exactly once**
- Find a similar path through the pull-down network that visits transistors **in the same order as the PUN**
- The resulting path corresponds to the order of the gates drawn on the stick diagram

Stick Diagrams

» $Y = \overline{A + BC}$

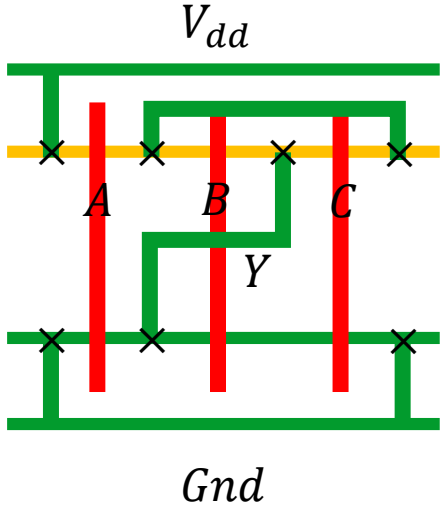


PUN Path: $V_{dd} \rightarrow \boldsymbol{A} \rightarrow N_1 \rightarrow \boldsymbol{B} \rightarrow Y \rightarrow \boldsymbol{C} - N_1$

PDN Path: $Gnd \rightarrow \boldsymbol{A} \rightarrow Y \rightarrow \boldsymbol{B} \rightarrow N_2 \rightarrow \boldsymbol{C} \rightarrow Gnd$

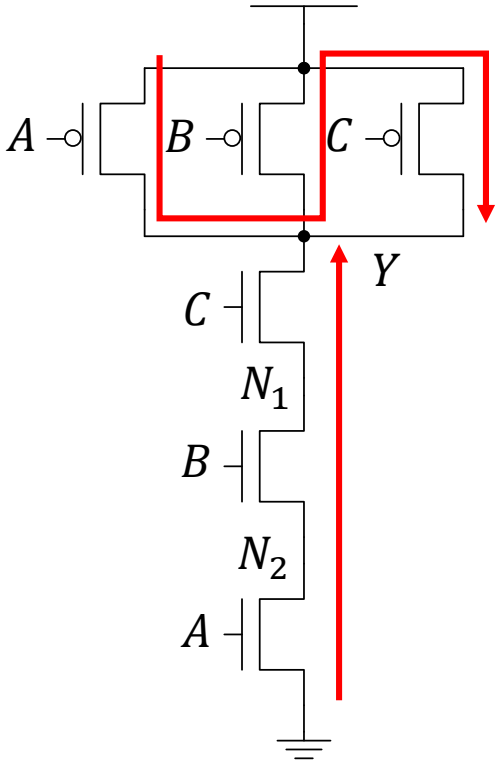
Note: Order of transistors is the same in both paths

Stick Diagram is drawn from the Euler path with gates in the same order



Stick Diagrams

» $Y = \overline{ABC}$

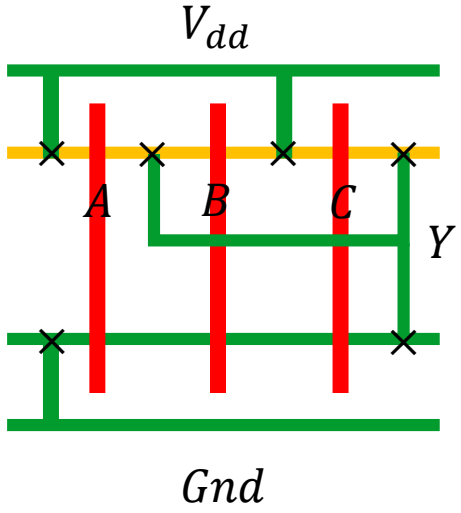


PUN Path: $V_{dd} \rightarrow \boldsymbol{A} \rightarrow Y \rightarrow \boldsymbol{B} \rightarrow V_{dd} \rightarrow \boldsymbol{C} - Y$

PDN Path: $Gnd \rightarrow \boldsymbol{A} \rightarrow N_2 \rightarrow \boldsymbol{B} \rightarrow N_1 \rightarrow \boldsymbol{C} \rightarrow Y$

Note: Order of transistors is the same in both paths

Stick Diagram is drawn from the Euler path with gates in the same order



Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Basic Layout Rules of Thumb

- Start with stick diagram
- Run metal lines for V_{dd} and Gnd horizontally at top and bottom of the cell (area of the layout)
- Run p+ and n+ diffusion just under and above V_{dd} and Gnd, respectively
- Run poly vertically and order transistors in a way that maximizes shared diffusion and shared poly
  - Use Euler's path
- Maximize number of contacts/vias to reduce resistance
- Limit routing with poly and diffusion
  - Use metal instead to reduce resistance

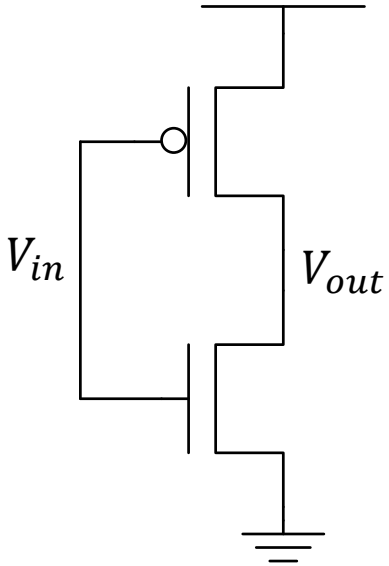
Basic Layout Rules of Thumb

- Place well and substrate connections close to V_{dd} and Gnd
- Use lower metal levels for shorter distance routing and higher metals for long distance
- Higher level metal lines should run parallel to each other, alternating the direction with each successive layer
- Minimize spacing while abiding by design rules
- Metal for V_{dd} and Gnd should be sized wider ($\geq 8\ \lambda$) than minimum
  - Have to support more current
  - Helps in reducing some noise on the supply lines

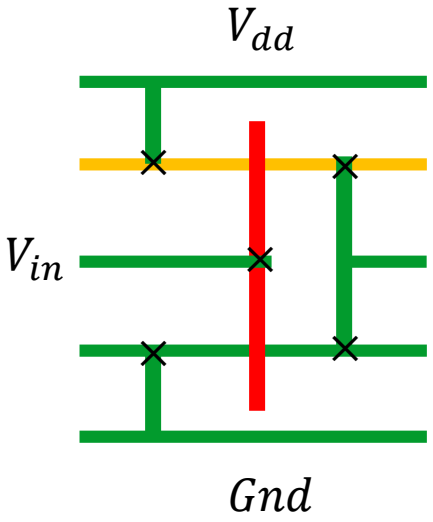
From Stick Diagram to Layout

» 4 views of same design:

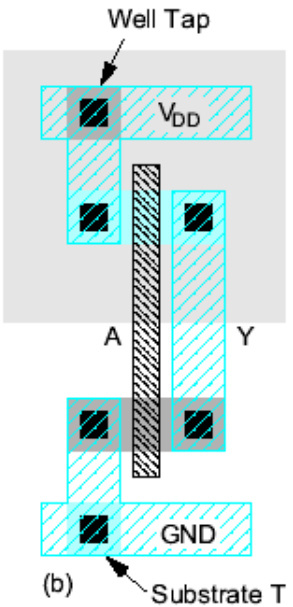
Schematic



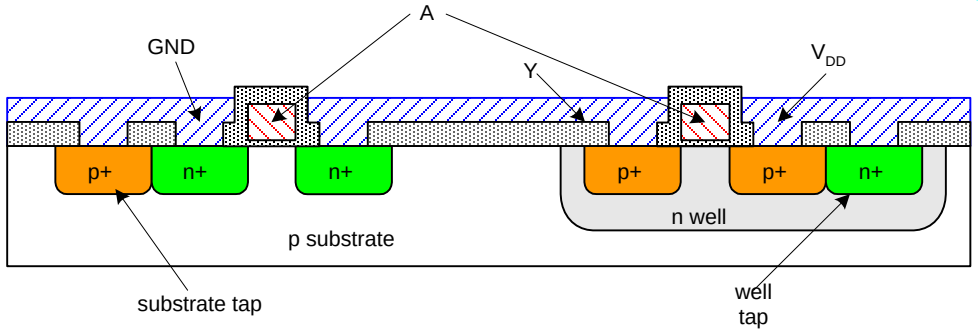
Stick Diagram



Layout



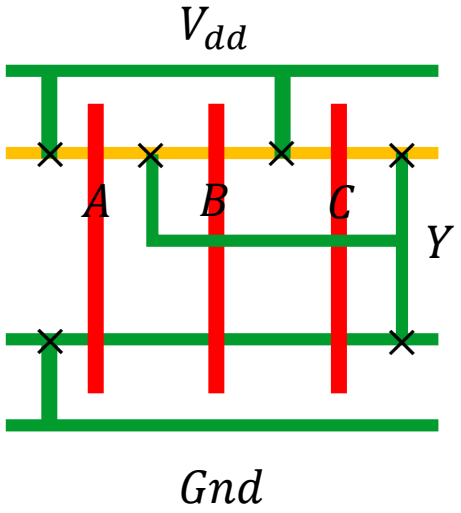
Physical Cross Section (Simplified)

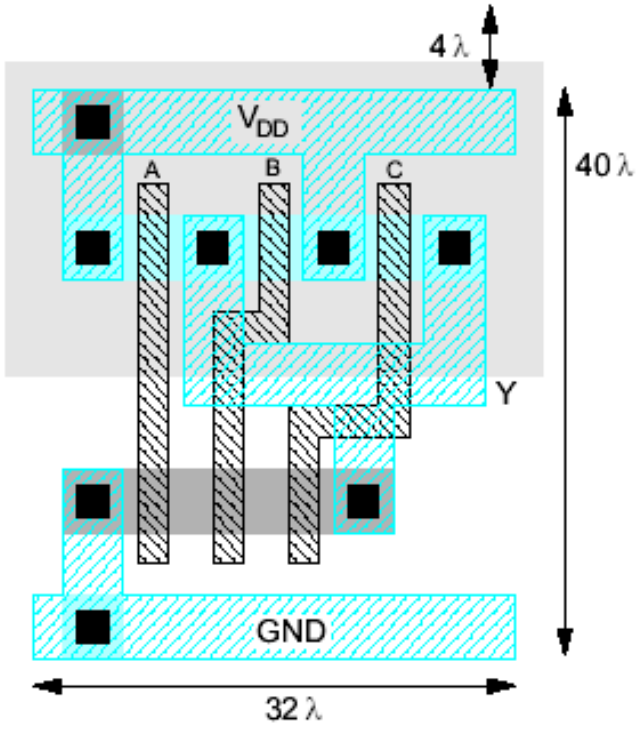


All spacing must follow design rules

From Stick Diagram to Layout

» 3-input NAND gate

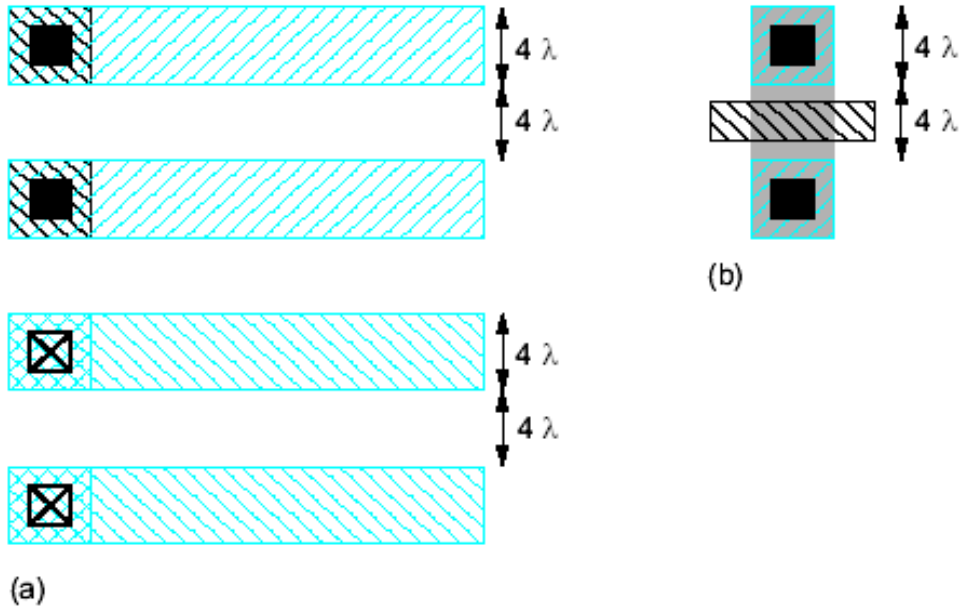




» Note: We could make the poly lines straight in t ıre bent to reduce the amount of n+ diffusion, which reduces capacitance and increases speed

Wiring Tracks

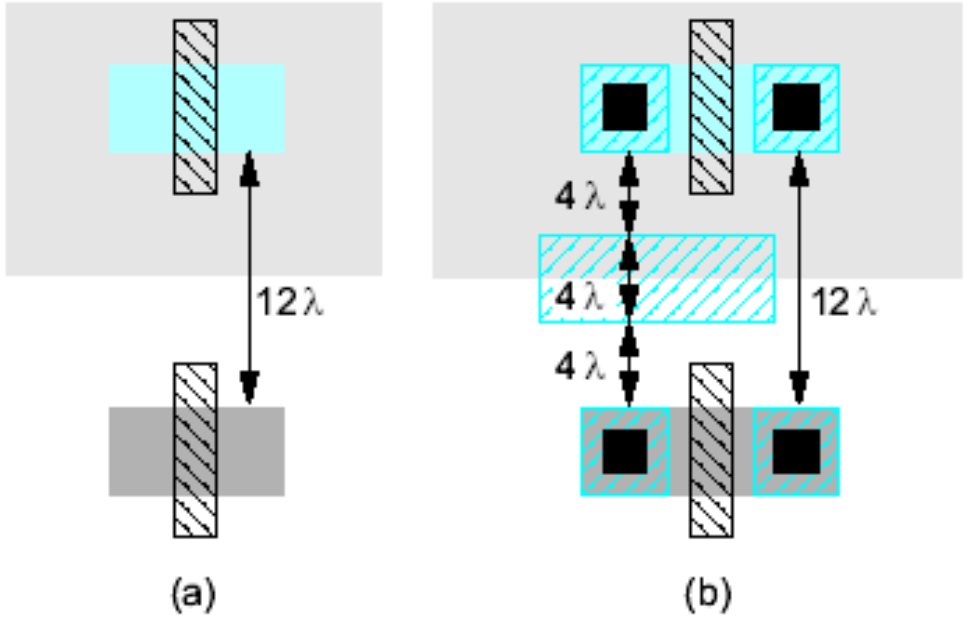
- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



- Can be used to approximate the area of a layout

Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



Optical Proximity Corrections

» Behavior of light causes undesired effects (e.g. rounding) that can be corrected by adding additional features to the photomasks