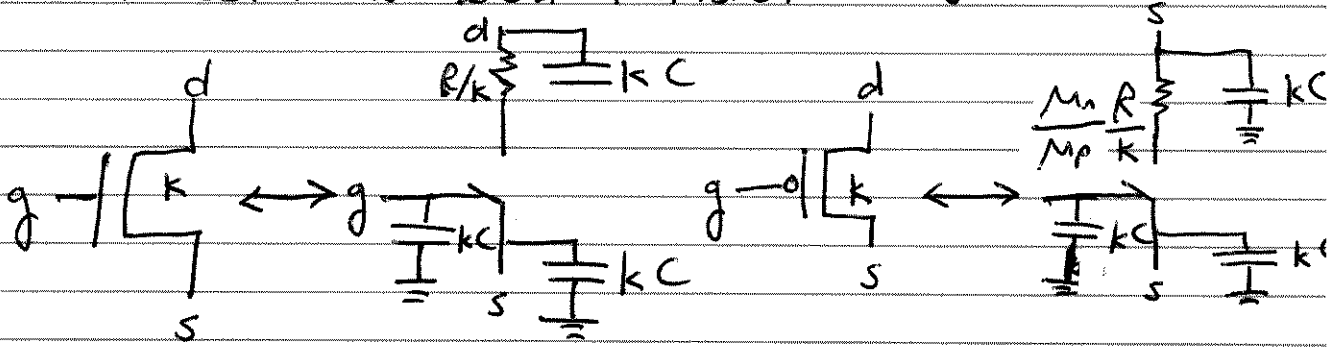
Recap: RC Delay Model

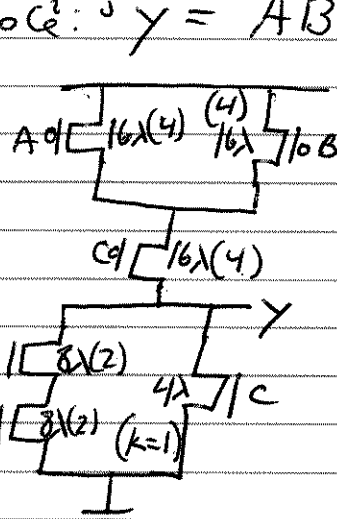
- Idea: ① estimate each transistor as

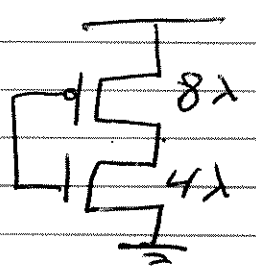


② Draw equivalent RC circuit for $t_{pr}, t_{pf}, t_{cr}, t_{cf}$ delays.

③ $\tau = \sum_i \sum_j R_j C_i$ where R_j is a resistor on the path from source to C_i

Example: $Y = \overline{AB+C}$, $\mu_n = 2\mu_p$

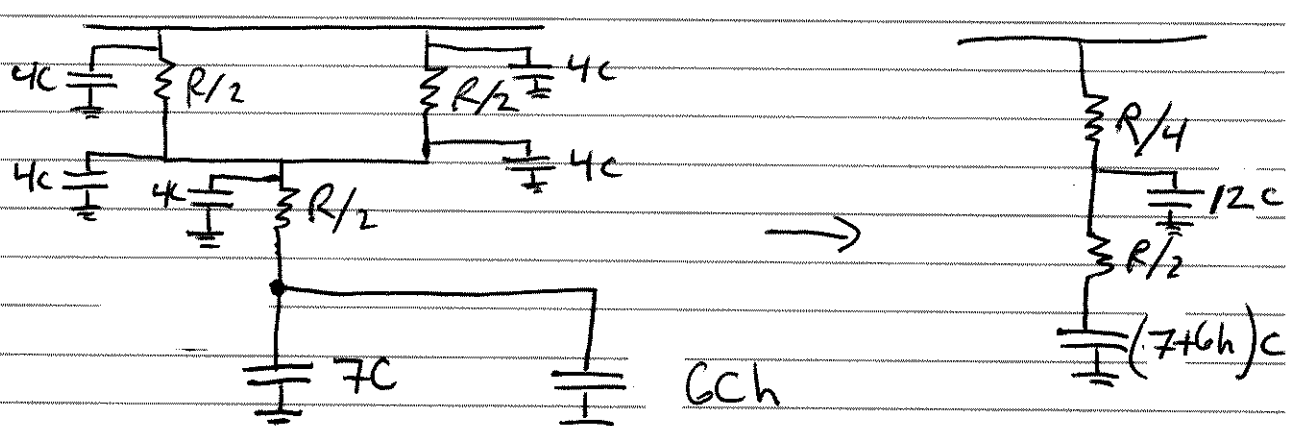




So, minimum width = 4λ

Find t_{cf} when output drives A input of h identical gates

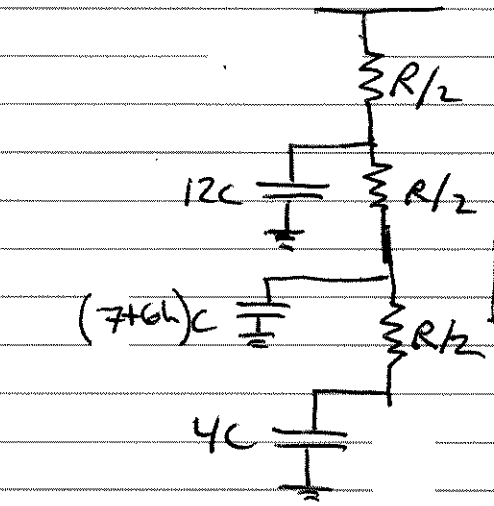
Best Case)



$$t_{cf} = \left(\frac{R}{4}\right)12C + \left(\frac{R}{4}+\frac{R}{2}\right)(7+6h)C = \boxed{\frac{3RC+21}{4}RC + \frac{9}{2}hRC}$$

Find t_{pr} when output drives A input of h identical gates

(worst-case)



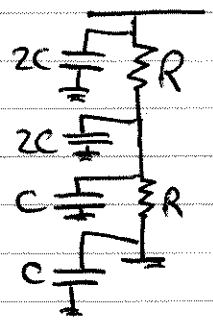
$$t_{pr} = \frac{R}{2}(12C) + \left(\frac{R}{2} + \frac{R}{2}\right)(7+6h)C$$

$$+ \left(R/2 + R/2\right)4C$$

$$= 6RC + 7RC + 6hRC + 4RC$$

$$\boxed{t_{pr} = (17+6h)RC}$$

Let τ' = the parasitic delay of the unit inverter (not driving any load)



$\rightarrow \tau' = 3RC$

Thus, $d \equiv \frac{t}{\tau} = f + p = gh + p$

f = "effort delay"

g = "logical effort" – ratio of gate input cap. to unit inverter

h = "electrical effort" or fanout $\rightarrow h = \frac{C_{out}}{C_{in}}$

p = "parasitic delay" – delay when no load is attached

for our AOI t_{pf}:

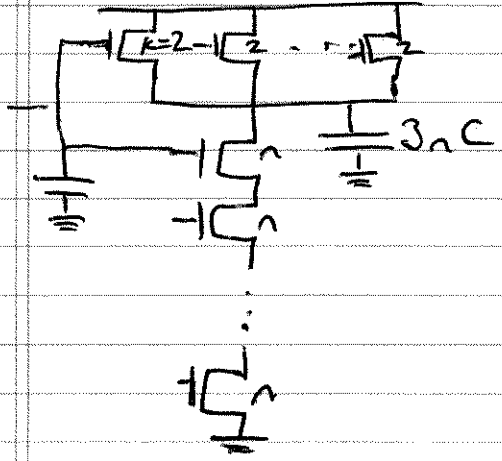
$$d = 2h + \frac{17}{3}$$

logical effort ← $2h$ → Fanout

$\frac{17}{3}$ → parasitic delay

Notice d is linear function of h $\rightarrow$ linear delay model

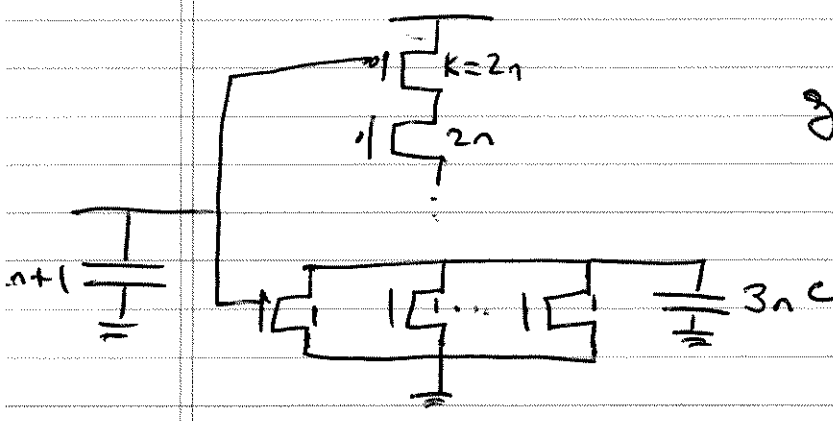
Logical effort and parasitic delay — example: n-input NAND Gate



$g = \frac{n+2}{3}$

$p = n$

n-input NOR gate:



$g = \frac{2n+1}{3}$

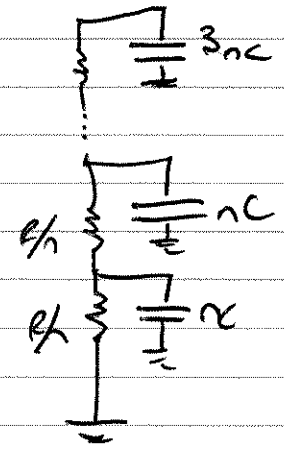
$p = n$

★ NOR gates are ≈ 2× slower than NAND gates

- What was wrong with our parasitic delay estimation?

  - need to include internal capacitances...

Example, n-input NAND where all inputs are 1 except bottom, which then rises...



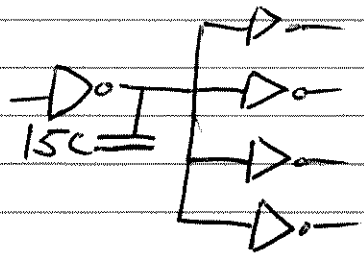
$$t_{par} = 3nRC + \overbrace{\sum_{i=1}^{n-1}\left(\frac{iR}{n}\right)(nC)}^{n(n+1)/2}$$

$$= \left(\frac{n^2}{2} + \frac{5}{2}n\right)RC$$

or $p = \frac{n^2+5n}{6}$

★ Actually quadratic in n, not linear → split big gates into smaller ones

FO4 delays



$t_p = 15RC$, $d = 5$

★ FO4 delays are roughly 1/3 to 1/2 of drawn channel length in picoseconds

for TSMC 180nm – FO4 ≈ 60-90 ps

Drive

- Redefine unit inverter to have input capacitance of 1

$$x = \frac{C_{in}}{\gamma} \sum \text{drive of a gate}$$

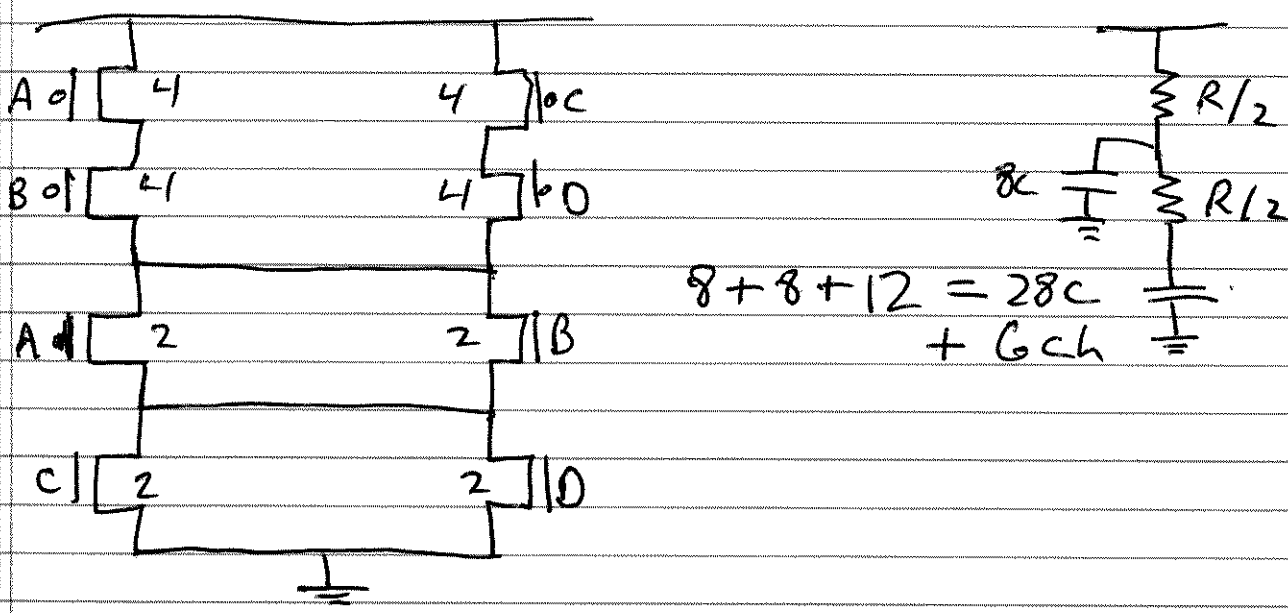
or

$$d = \frac{C_{out}}{x} + p$$

Class exercise

- Calculate the rising propagation delay of $\overline{(A+B)(C+D)}$ w/ fanout of 4.
- What is the logical effort?
- What is the parasitic delay?
- What is the drive if minimum sizing is used?

Assume $W_{min} = 4\lambda$, $\mu_n = 2\mu_p$

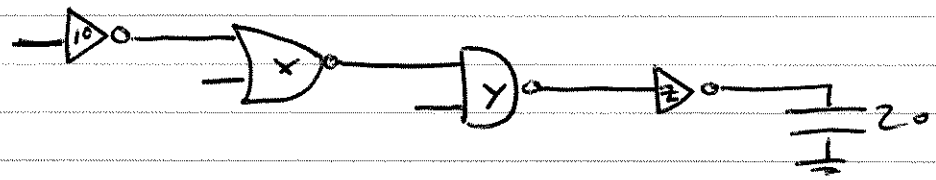


Worst-case: A=1, B=0, C=0, D=0

$$t_{pf} = \frac{f}{2}(8c) + R(28c + 6ch) = 64RC + 32RC$$

- logical effort $= \frac{6}{3} = 2$
- parasitic delay $= \frac{32}{3}$
- drive $= \frac{C_{in}}{3g} = \frac{2}{3(2)} = \frac{1}{3}$

Delay in Multi-stage Networks



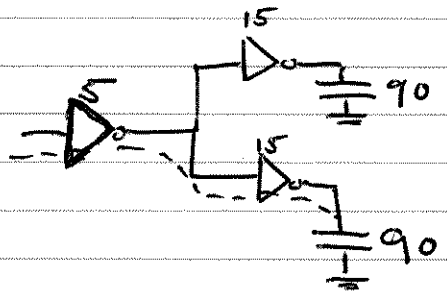
$g_1 = 1 \quad g_2 = 5/3 \quad g_3 = 4/3 \quad g_4 = 1$

$h_1 = x/10 \quad h_2 = y/x \quad h_3 = z/y \quad h_4 = 20/z$

Definitions: Path logical effort $\rightarrow G \equiv \prod g_i$

Path electrical effort $\rightarrow H \equiv \dfrac{C_{out(path)}}{C_{in(path)}}$

Path effort $\rightarrow F \equiv \prod f_i = \prod g_i h_i$



$G = 1 \times 1 = 1$

$H = \dfrac{90}{5} = 18$

$F = \left(1 \times \frac{30}{5}\right)\left(1 \times \frac{90}{15}\right) = 36 \neq GH!$

Branching effort $\rightarrow b \equiv \dfrac{C_{onpath} + C_{offpath}}{C_{onpath}}$

Path branching effort $\rightarrow B \equiv \prod b_i$

$$\boxed{F = GBH}$$

Path Delay $\rightarrow D \equiv \sum d_i = D_F + P$

$D_F \equiv \sum f_i \rightarrow$ path effort delay

$P \equiv \sum p_i \rightarrow$ Path parasitic delay

Path effort delay is minimized when $f_i = f_j \; \forall_{i,j}$

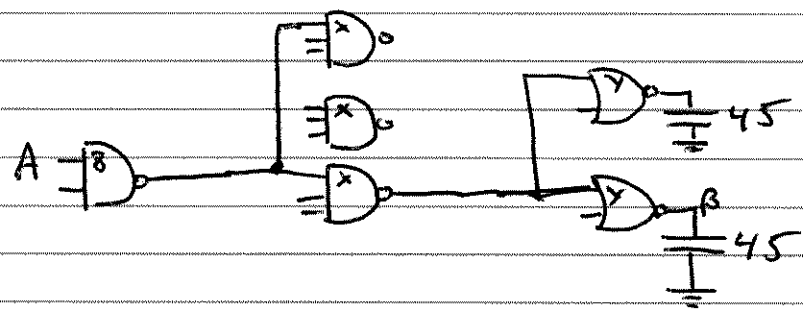
or, $\hat{f} = F^{1/N}$

Minimum possible delay of N-stage path is

$$\boxed{D = NF^{1/N} + P}$$

Capacitance transformation formula:

$$C_{in_i} = \frac{C_{out_i} \times g_i}{\hat{f}}$$ } Best input capacitance for a gate given its output capacitance



$G = \left(\frac{4}{3}\right)\left(\frac{5}{3}\right)\left(\frac{5}{3}\right) = 100/27$

$H = 45/8$

$B = \left(\frac{3x}{x}\right)\left(\frac{2y}{y}\right) = 6$

$F = GBH = 125$

Best stage effort is $\hat{f} = 125^{1/3} = 5$

$P = 2+3+2 = 7$

$D = N\hat{f} + P = 3\times 5 + 7 = 22$ or 4.4 FO4 delays

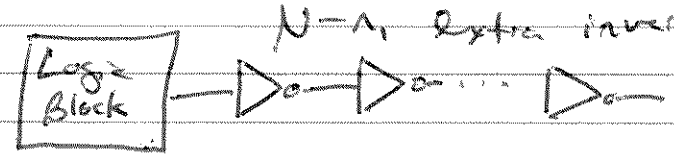
Now find input capacitances

$$y = C_{in_3} = \frac{45(5/3)}{5} = 15$$

$$x = C_{in_2} = (15+15)\times(5/3)/5 = 10$$

So, we can size transistors according to C_{in} and constraint of equal rise/fall times

What's the best # of stages?



n_1 stages

path effort F

$$D = NF^{1/N} + \sum_{i=1}^{n_1} p_i + (N-n_1)p_{inv}$$

Let $\rho = F^{1/N}$

$$\frac{\partial D}{\partial N} = 0 \rightarrow p_{inv} + \rho(1-\ln\rho) = 0$$

$\rho = 2.71828$ (e) with $p_{inv} \approx 0$

or $\rho = 3.59$ with $p_{inv} = 1$

So, a path has least delay when

$$N = \log_p F$$